Low Power Full Swing Sram Architecture with Power Gating

A. ASHNA[1], M. FAROUS KHAN[2], T. G. KARTHIKEYAN[3], R. ARUN RAJ[4]
[1] *Assistant Professor ECE, Sri Ramakrishna Institute of Technology, Coimbatore, India*
[2,3,4] *B.E Final year ECE, Sri Ramakrishna Institute of Technology, Coimbatore, India*

Abstract- The attacks in the field of power analysis is becoming a major threat to security systems by triggering secret data extraction using side channel leakage information .Nowadays almost every Memory in Embedded systems, is now utilizing 8T and 6T SRAM cells, it is one of the major components in many systems .Generally SRAM cells are likely to suffer from side channel leakage power attacks .To overcome this types of attacks, we proposed a 9T SRAM which has one additional transistor compared to 8T cell and incorporates three more transistor when compared to 6T SRAM cell which greatly improves the number of operations per second in SRAM interms of speed and the power is also decreased The cells were implemented in 125nm technology on Tanner EDA tool.

Indexed Terms - Static Random Access Memory (SRAM), Side Channel Attacks (SCA), Leakage Power Analysis (LPA)

I. INTRODUCTION

A SRAM mobile encompass a latch, therefore the mobile records is kept as long as strength is grew to become on and refresh operation isn't required for the SRAM cell. SRAM is particularly used for the cache memory in microprocessors, mainframe computer systems, engineering workstations and memory in hand-held devices due to excessive space and occasional power consumption. Each bit in an SRAM is saved on four transistors that shape two pass-coupled inverters. The electricity intake and velocity of SRAM are vital difficulty that has cause more than one designs with the cause of minimizing the electricity consumption at some stage in each read and write operations. High-overall performance on chip caches is a vital component inside the memory hierarchy of modern computing structures. In this method every NMOS and PMOS transistor within the common sense gates is break up into two transistors are known as Stack Technique, Leakage modern-day flowing via the NMOS transistor stack reduces because of the growth inside the source to substrate voltage in the pinnacle NMOS transistor and also due to the drain to supply voltage within the bottom NMOS transistor. This reduces the strength dissipation in logic circuits.

SRAM reminiscence cellular consumes lower energy during read and writes operations compared to 6T conventional circuit. The potential of the cellular to write nicely and to have enough study noise margin may be very critical for sub threshold location. We take a look at lots of such necessities for a success operation. Also, a new 9T SRAM combining the advantages of those circuits is proposed in the paper. A nine transistors (9T) SRAM cell configuration is proposed on this paper, which is amenable to small function sizes encountered within the deep sub-micron/Nano CMOS levels. Compared with the 8T and 10T cells of [1] and [2], the 9T scheme gives widespread blessings in terms of power intake. The traditional six transistor (6T) SRAM cell shows terrible balance at very small characteristic size with low electricity supply. During the read operation, voltage division between the get entry to and driver transistors causes the examine stability to be very low. Hence on this paper, a 9T SRAM cellular is proposed for excessive study balance and coffee power intake. The proposed cellular makes use of single bit-line (BL) for write operation, ensuing in discount of dynamic power consumption. During examine operation, the facts garage nodes are completely isolated from the bit lines, accordingly ornamental the read static noise margin. Hence in this paper, a 9T SRAM mobile is proposed for high read stability and low power consumption [5]. The proposed cellular makes use of unmarried bit-line (BL) for write operation, ensuing in reduction of dynamic power intake. During examine operation; the data is completely remoted from the bit line, as a consequence enhancing the study static noise margin.

II. CONVENTIONAL 6T SRAM CELL

Traditional 6T SRAM Cell indicates the conventional 6T SRAM cell with transistor sizing in 125 nm CMOS technology. The schematic diagram of 6T SRAM cell is shown in Fig.1. Access to the mobile is enabled by the phrase line (WL) which controls the 2 get entry to transistors, in turn, control whether or not the cellular need to be related to the bit strains: BL and BLB. They are used to transfer information for both read and write operations.

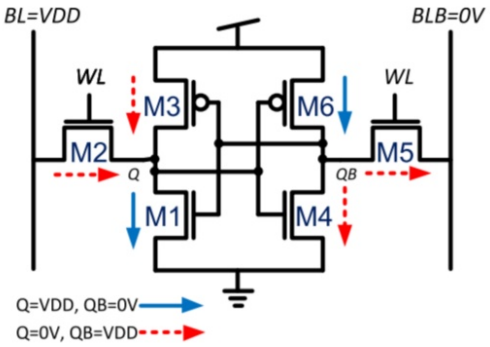

Fig 1: 6T SRAM CELL

While it is no longer strictly vital to have bit lines, both the sign and its inverse are typically provided since it improves noise margins.

III. PROPOSED 9T SRAM CELL

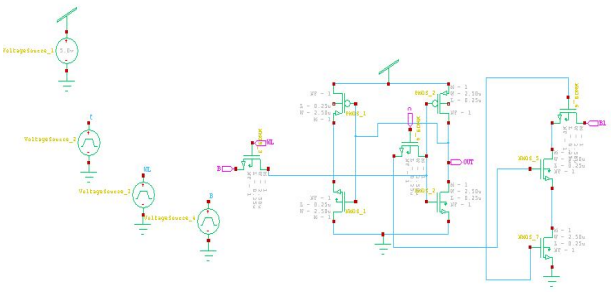

Fig 2: Schematic of 9T SRAM

This circuit shows decreased leakage power and more desirable records stability. The 9T SRAM cellular absolutely isolates the facts from the bit lines during a read operation. The idle 9T SRAM cells are located right into a excellent cutoff sleep mode, thereby lowering the leakage electricity intake in comparison to the same old 6T SRAM cells.

A. Bit Line Scheme:

The top-quality transistor sizing for this 9T SRAM cellular thinking about stability, energy intake and postpone. A write bit line balancing scheme is proposed to reduce the leakage contemporary of the SRAM cell. A 9T structure is to enhance the SNM by way of setting apart the read get entry to systems of the original 6T cell, thus making the study SNM same to the hold SNM. An modern precharging and bit line balancing scheme for writing operation of the 9T SRAM mobile is likewise proposed for optimum standby strength financial savings in an SRAM array.

B. Stack Technique:

Power consumption has end up a important design concern for many VLSI systems [12]. Leakage present day flowing via the NMOS transistor stack reduces due to the increase in the supply to substrate voltage inside the top NMOS transistor and also due to an increase inside the drain to source voltage in the backside NMOS transistor. This reduces the energy dissipation in good judgment circuits. In this technique every NMOS and PMOS transistor inside the logic gates are split into transistors. A state with more than one transistor is off situation from a course from supply voltage to ground direction consist of much less leakage in comparison to the simplest one transistor off situation from a direction from deliver voltage to ground direction.

C. Improve Read Stability

The statistics in a conventional 6T SRAM cellular as proven in determine.1, is maximum vulnerable to external noise due to the direct get right of entry to of the statistics garage nodes by using the get admission to transistors (N3 and N4) related to bit line (BL) and bit line bar (BLB) respectively[9]. During read operation, the voltage department among the access transistors and pass coupled inverters °fluctuate the storage node voltage, ensuing in detrimental examine operation. The 9T SRAM cellular in determine has an advanced static noise margin (SNM) as compared to conventional 6T SRAM cell. The higher sub-circuit of the reminiscence mobile is largely a 6T SRAM cellular (composed of N1, N2, N3, N4, P1, and P2). The two write access transistors (N3 and N4) are controlled by a write signal (WR). The facts are saved inside this upper reminiscence sub circuit. The decrease sub-circuit of the brand new cellular is composed of the bit-line get right of entry to transistors (N5 and N6) and the read get admission to transistor (N7). The operations of N5 and N6 are controlled via the statistics stored within the mobile.

N7 is controlled with the aid of a separate study sign (RD). This structure absolutely isolates the bit lines from the data storage nodes in the course of examine operation hence improving the static noise margin (SNM).But during write operation it utilizes both bit line(BL) and bit line bar (BLB) capacitances for charging and discharging, resulting in improved dynamic strength consumption. In this 9T SRAM cell, the get admission to transistor N4 is located within the comments route and most effective access transistor N3 is hooked up to bit line (BL) to store information in the cellular. Hence simplest one bit line capacitance (BL) can be charged and discharged in the course of write operation which ends up in primary discount in dynamic energy ingestion and on the same time the records balance of the 9T SRAM cellular as in is likewise maintained. The top sub circuit of the proposed cellular has 6 transistors composed of N1, N2, P1, P2, N3 and N4. The 9T SRAM mobile proven in determine has write get admission to transistors organized by a write sign (WR) related to bit line (BL) and bit line bar (BLB). The projected cell entails of 1 write get admission to transistor (N3) coupled to BL, managed through a write sign (WR), and one study and keep get entry to transistor (N4) managed via a manipulate sign (CTRL). The decrease sub circuit of the planned cellular is accumulated of bit line get right of entry to transistor (N5), bit line bar access transistor (N6) and examine get entry to transistor (N7) controlled by means of a examine signal (RD) as proven in figure. 3 .During a write operation, WR signal is maintained at a excessive voltage (1" stage). RD and CTRL alerts are sustained at a low voltage (0" stage). Hence the access transistors N4 and N7 are cut OFF and the write get entry to transistor N3 is became ON. To write a 1" to Node 1, BL is charged and 1" is pressured to Node X thru N3. This turns ON the transistor N2, forcing zero" into Node 2. This turns ON the transistor P1, forcing BL is discharged. Hence, to recognize a write operation charging /discharging of simplest bit line (BL) is developed.

D. Simulation and Discussion:

All the circuits have been simulated the use of BSIM 3V3 125nm technology on Tanner EDA tool with supply voltage ranging. The basic SRAM shape can be considerably optimized to reduce the postpone and strength on the price of a few location overhead. The optimization begins with the layout and layout of the RAM cell, that's undertaken in consultation with the method technologists. For the most element, the thesis assumes that a ram cellular has been effectively designed and appears at how to placed the cells together efficiently

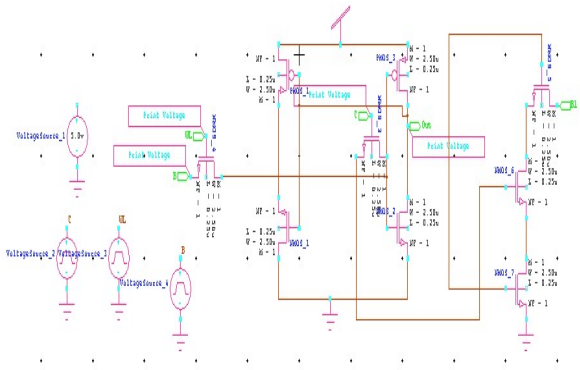

Fig 3: Schematic of 9T SRAM

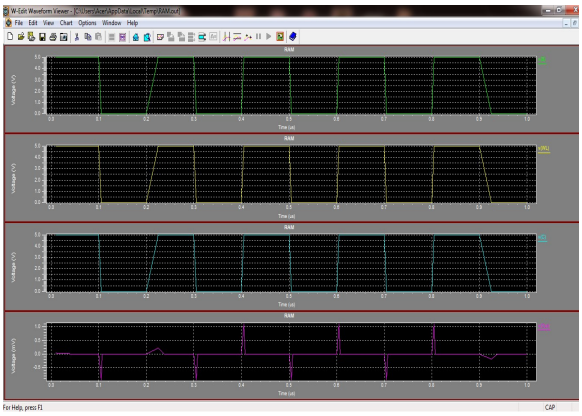

Fig 4: Waveform of 9T SRAM

From figure 3, WL is the Word Line , BL is the Bit Line and CTRL is the control transistor that is used to control the input signals coming from the word line. The Word line is used to set the input signal and Bit line acts has an iteration signal controller, that determines which signal of WL to be sent to the cross coupled inverters .The waveform form figure 4 ,when WL and B are High the control (CTRL) transistor will be also High . The output is taken at one end of the cross coupled inverter and if the CTRL is also High means it sends the signal to series NMOS architecture from Fig 3.

IV. FURTHER WORKS TO BE DONE

The various parameter calculations such has Power, Delay and temperature of the above shown 9T SRAM cell design is to be calculated in comparison with the existing 6T and 8T SRAM cells.

E. POWER ANALYSIS:

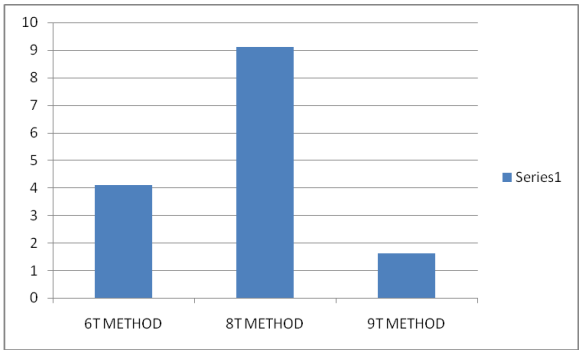

TABLE 2: POWER MEASURMENT FOR TRANSISTORS

S.NO	METHODS	POWER MEASUREMENT
1	6T METHOD	4.099
2	8T METHOD	9.1214
3	9T METHOD	1.603

F. DELAY ANALYSIS:

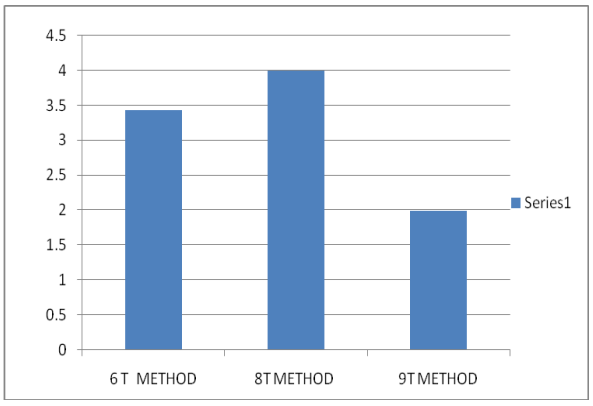

TABLE 2: DELAY MEASUREMENT FOR TRANSISTORS

S.NO	METHODS	DELAY MEASUREMENT
1	6 T METHOD	3.4291
2	8T METHOD	4
3	9T METHOD	1.996

V. CONCLUSION

Memories in Embedded systems implemented with 6T SRAM macros occupy a large portion of cryptographic systems and may hold secret data these require special design steps to overcome the leakage power attacks. In this brief, we provide an in-depth analysis of the leakage dependence on the stored data of a 6T SRAM array. A leakage power attack is illustrated on a 6T SRAM cell, and achieved successful data extraction through leakage current measurements to prove its unreliability for security applications. To generate a leakage power attack resilient memory array, an 9T SRAM cell was proposed to reduce the correlation between the content of the cell and its leakage power dissipation. Using a sample leakage power attack algorithm, the 9T cell will be proven to be resilient to leakage power attacks when compared to the existing methodology.

ACKNOWLEDGMENT

Sincere thanks to our guide Ms. A. Ashna, Assistant Professor ECE, Sri Ramakrishna Institute of Technology and our beloved DR. H. Mangalam HOD of ECE, Sri Ramakrishna Institute of Technology who were all with us during tough times and guided us upon the completion of this project.

REFERENCES

[1] P. Kocher, J. Jaffe, B. Jun, and P. Rohatgi, “Introduction to differential power analysis,” J. Cryptograph. Eng., vol. 1, no. 1, pp. 5–27,Apr. 2011.

[2] S. Mangard and A. Y. Poschmann, “Constructive Side-Channel Analysis and Secure Design”. Cham, Switzerland: Springer-Verlag, 2015.

[3] M. Alioto, L. Giancane, G. Scotti, and A. Trifiletti, "Leakage power analysis attacks: A novel class of attacks to nanometer cryptographic circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 2,pp. 355–367, Feb. 2010.

[4] M. Alioto, S. Bongiovanni, M. Djukanovic, G. Scotti, and A. Trifiletti, "Effectiveness of leakage power analysis attacks on DPA-resistant logic styles under process variations," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 2, pp. 429–442, Feb. 2014.

[5] A. Moradi, "Side-channel leakage through static power," in Proc. Int. Workshop Cryptograph. Hardw. Embedded Syst. Berlin, Germany:Springer-Verlag, 2014, pp. 562–579.

[6] S. M. D. Pozo, F. X. Standaert, D. Kamel, and A. Moradi, "Side-channel attacks from static power: When should we care?" in Proc. Design Autom. Test Europe Conf. Exhib. (DATE), Mar. 2015, pp. 145–150.

[7] M. Neve, E. Peeters, D. Samyde, and J.-J. Quisquater, "Memories:A survey of their secure uses in smart cards," in Proc. 2nd IEEE Int.Secur. Storage Workshop (SISW), Oct. 2003, p. 62.