Harmonic Analysis of Embedded Enhanced-Boost Z-Source Inverter

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Abstract -- This paper proposes a modified inverter topology called Embedded Enhanced-Boost Z-Source Inverter (EEB- ZSI). Compared with the prior-art Enhanced-Boost Z-Source Inverter (EB-ZSI), the proposed topology features that the dc sources like PV panels can be embedded into a symmetrical impedance network. In this way, the dc current becomes continuous. More importantly, the voltage stress across the switching devices is lower, while a large conversion ratio is maintained. The proposed Z-source inverter is benchmarked with selected topologies in terms of the conversion ratio, voltage gain, and stresses on the devices. Simulation and experimental results are provided to validate the analysis.

Indexed Terms: Z-source inverter, embedded Z-source, high conversion ratio, continuous input current

I. INTRODUCTION

Traditional Voltage Source Inverters (VSIs) are widely used in industrial applications, e.g., motor drives, distributed power systems, and hybrid electric vehicles [1], which are typically in the buck operation mode. Generally, a dc-dc boost converter is used to achieve a high conversion of the dc voltage, which is then fed to an inverter. However, this two- stage power conversion increases the system cost and lowers the efficiency. The Z-source inverter (ZSI) [2] shown in Fig.1 as a single-stage conversion, can effectively tackles those issues. Hence, many efforts have been made in recent years to enhance the performance of Z-source inverters by means of topological innovations and advanced control strategies.

Nonetheless, in order to increase the boost capability, more passive components (e.g., inductors and capacitors) should be added into the classic Z-source network shown in Fig. 1. For instance, a Switched-Inductor (SL) Z-source inverter (SL-ZSI) [3], as shown in Fig. 2, adopts two SL cells to replace the two inductors (L_1 and L_2) in traditional Z-source inverter, and thus leading to a higher conversion ratio. Based on the SL- ZSI topology, modified topologies were developed to further increase the boost ratio. For instance, according to the quasi Z-source inverter, two SL qZSI topologies were proposed in [4] and [5].

In addition, the boost capability can be improved by using more cascaded networks. In [6] and [7], the extended-boost ZSI topologies are called diode-assisted or capacitor-assisted converters for high boost ratios. A new family of high-boost ZSIs with switched impedance is presented in [8] and [9]. More specially, in [8], a topology with a switched impedance network (EB-ZSI) was introduced, as shown in Fig. 3, which can achieve an even higher boost ratio due to the shorter shoot-through duration and a larger modulation index. However, the inverter volume also increases because of the extra inductors and/or capacitors.

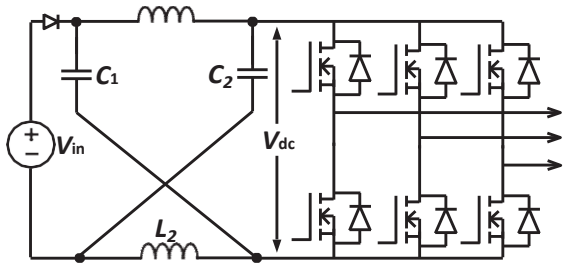

Fig. 1: Classic three-phase Z-source inverter, where V_{in} is the input DC voltage and V_{dc} is the DC-link voltage.

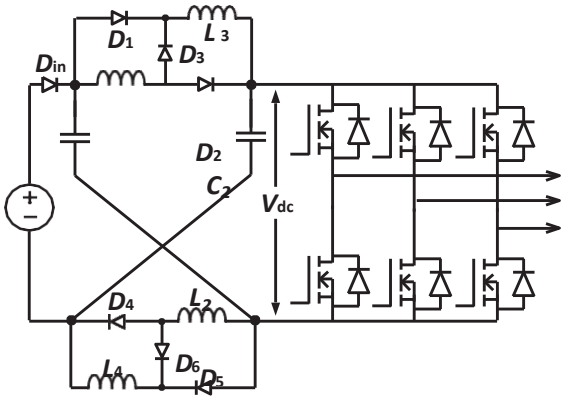

Fig. 2: Three-phase switched-inductor Z-source inverter [3].

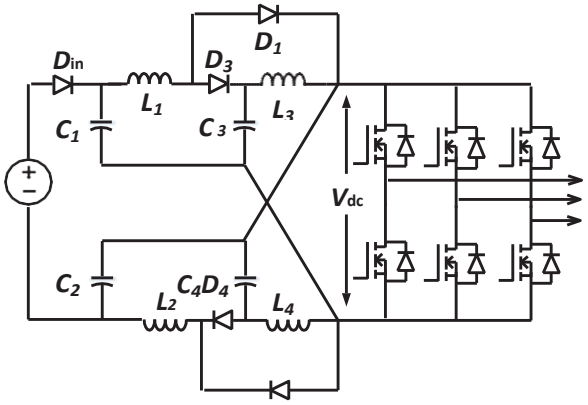

Fig. 3: Enhanced-boost Z-source inverter [8].

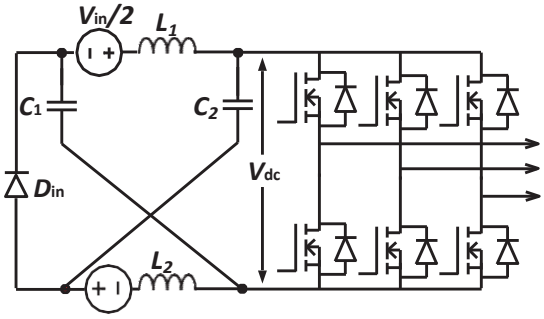

Fig. 4: Parallel-embedded Z-source inverter [10].

Additionally, the dc currents of ZSIs are normally chopped due to the shoot-through operation. To address this problem, a number of embedded ZSI topologies were proposed [10], [11], which also achieve lower capacitor voltage ratings. A typical parallel-embedded Z-source inverter (E-ZSI) is exemplified in Fig. 4, where it can be observed that two dc sources (e.g., PV panels) are directly connected in series with the inductors (i.e., (L_1 and L_2)) of the classic ZSI in Fig. 1. This topology is especially suitable for PV or fuel cell systems.

Inspired by the above, a new topology is proposed in this paper by modifying the embedded Z-source and switched Z-source, where Z represents impedance inverters. The pro- posed topology can achieve continuous dc source currents and also reduce the voltage stresses with a relatively large boost factor. In Section II, the operation principle of the proposed topology is presented. Comparisons with the con- ventional switched impedance networks and the embedded ZSIs are performed, and benchmarking results are given in Section III. Simulation and experimental results are provided. in Section IV, which verify the improved performance of the proposed Z-source topology in terms of continuous dc currents and also reduced voltage stresses. Finally, the paper is concluded in Section V.

II. OPERATION PRINCIPLE OF THEPROPOSED EEB-ZSI TOPOLOGY

Fig. 5 shows the topology of the proposed Embed- ded Enhanced-Boost Z-Source Inverter (EEB-ZSI), which demonstrates two symmetrical Z-source networks with em- bedded dc sources. The operation principle of the EEB-ZSI is the same as that of the conventional ZSI, there are two operating states, i.e., the shoot-through state and non-shoot- through state.

The equivalent circuits of the proposed Z-source converter in the shoot-through state and non-shoot-through state are shown in Figs. 6 and 7, respectively. It is assumed that all capacitors (and inductors) in the proposed topology are identical. Moreover, the dc sources in the two Z-impedance network sare the

same voltage of $0.5V_{in}$, with V_{in} being the input voltage of the dc source before splitting. According to the topological symmetry, it can be obtained that

$$V_{C1}=V_{C2}$$
$$V_{C3}=V_{C4}$$

in which V_C ,V_C , V_C , and V_C

age across the capacitor C_1, C_2, C_3, and C_4. As mentioned above, the operation can be separated into two states:

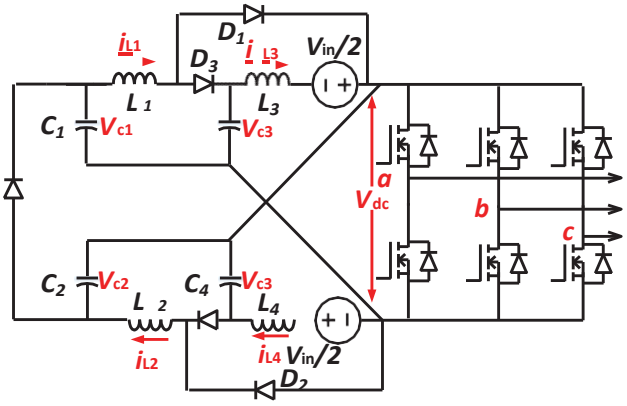

Fig. 5: Proposed three-phase embedded enhanced-boost Z-source inverter

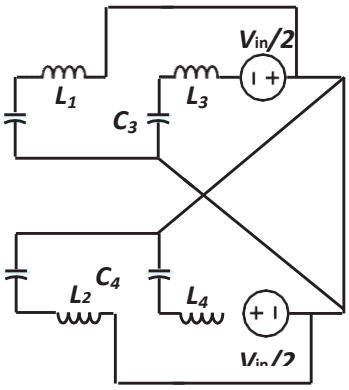

Fig. 6: Shoot-through state of the proposed Z-source inverter

A. Shoot-Through State:

As shown in Fig. 6, $D_1$and D_2 are ON with D_3, D_4, and D_{in} being reverse-biased in the shoot-through state. Additionally, L_1 and L_2 are in parallel with C_1 and C_2, respectively. Then, it can be obtained that

$$V_{C1}=V_{C2}=V_{L1}=V_{L2} \qquad (3)$$

where V_{L1} and V_{L2} are the voltage of the inductor L_1 and L_2, respectively.

According to the Kirchhoff's voltage law, the voltages on the inductors L_3 and L_4 can be expressed as

$$V_{L3} =V_{C3} +0.5V_{in} \qquad (4)$$
$$V_{L4} = V_{C4} + 0.5V_{in} \qquad (5)$$

with V_L3, and V_L4 being the inductor voltages in the shoot-through state.

B. Non-Shoot-Through State:

As shown in Fig. 7, D, D, and D are ON, and D and 2 are OFF. In one switching cycle, the inductor average voltage should be zero, and then applying the volt-second balance principle to all the inductors gives

$$DV_{L1}+ (1-D)V_{L1\text{-}NON}= 0 \qquad (6)$$
$$DV_L3 + (1-D)V_L3\text{-}NON=0 \qquad (7)$$

are the corresponding volt-

where V_L1-NON and V_L3-NON represent the inductor voltage on L_1andL_3,respectively,duringthenon-shoot-throughstate,

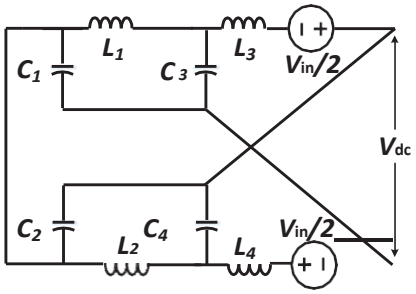

Fig. 7: Non-shoot-through state of the proposed Z-source inverter.

and D is the duty cycle. With (3), (4), (6) and (7), V_L1-NON and V_L3-NON can be solved as

$$V_{L1\text{-}NON}=-\frac{D}{1-D}V_{C1} \qquad (8)$$

$$V_{L3\text{-}NON}=-\frac{D}{1-D}(V_{C3}+0.5V_{in})$$

Furthermore, according to Fig. 7, the following can be obtained by applying the Kirchhoff's voltage law:

$$V_L1\text{-NON}+V_C3-V_C1=0 \quad (10)$$

$$V_L1\text{-NON}+V_L3\text{-NON}-0.5V_{in}+V_C2=0 \quad (11)$$

$$V_L1\text{-NON}-0.5V_{in}+V_{dc}-V_C3=0 \quad (12)$$

Accordingly, the capacitor voltage V_C3 and the peak dc-link voltage V_{dc}^{p} can be expressed as

in which G is the buck-boost factor, M is the modulation index, and V_{dc} is the average dc-link voltage. The buck-boost factor can be expressed with respect to the modulation index M as

$$M\,2$$

$$tt=MB = 2\overline{M\,2-1}(13)$$

III. COMPARISON OF THE PROPOSED EEB-ZI WITH OTHER TOPOLOGIES

A detailed comparison of the ZSI, E-ZSI, EB-ZSI and EEB-ZSI is performed, and the benchmarking results are summarized in Table I. Fig. 8 shows the relationship between the shoot-through duty ratio and the boost factor among these topologies. Although the boost factor of the proposed EEB- ZSI is slightly lower than the conventional EB-ZSI, it is much higher than the ZSI and the E-ZSI, as observed in Fig. 8. In addition, Fig. 9 compares the voltage gains of the selected topologies in respect to the modulation index.

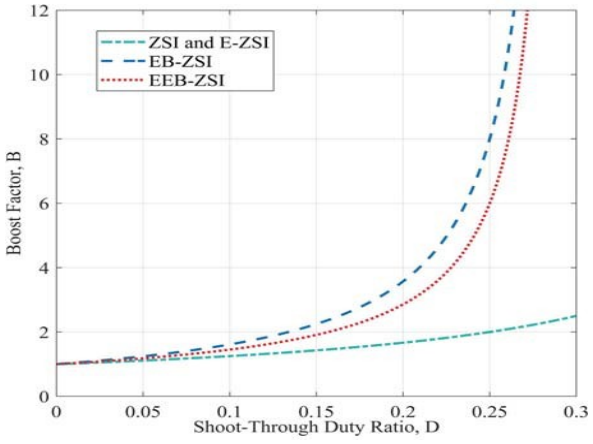

Fig. 8: Boost factor comparison of the three Z-source inverters (i.e., the ZSI, E-ZSI, and EB-ZSI) with the proposed inverter topology.

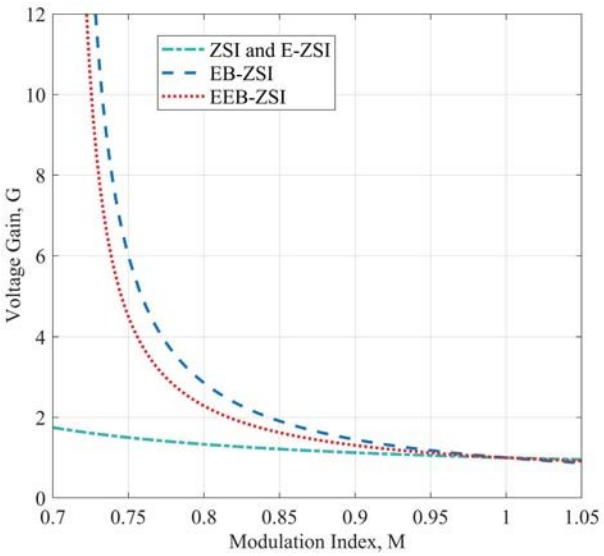

Fig. 9: Voltage gain comparison of the three Z-source inverters (i.e., the ZSI, E-ZSI, and EB-ZSI) with the proposed inverter topology

It can be seen in Fig. 9 that the voltage gain of the proposed impedance-source topology is higher than the conventional embedded ZSI and the classic ZSI. However, it achieves a slightly lower voltage gain when comparing with the EB- ZSI. Nevertheless, the proposed topology can achieve lower voltage stresses, as shown in Figs. 10 and 11. The voltage stresses are defined as the ratio of the peak dc-link voltage tand capacitors voltage ot the minimum dc voltage. It can be seen in Fig. 10 that the proposed EEB-ZSI has a better performance compared with other topologies in terms of voltage stresses over the power switches. The power switch stress of the proposed EEB-ZSI is almost the same as the EB- ZSI but much lower than the ZSI and E-ZSI for the same voltage gain, as observed in Fig. 10. In addition, Fig. 11 shows that the capacitor voltage stress of the proposed EZ- ZSI is less than the EB-ZSI, and thus, the capacitors with lower ratings can be used to reduce the cost and size for

TABLE I
BENCHMARKING OF SELECTED IMPEDANCE-SOURCE INVERTERS.

	ZSI[2]	E-ZSI[10]	EB-ZSI[8]	EEB-ZSI
B	$\frac{1}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{2D^2-4D+1}$	$\frac{1-D}{2D^2-4D+1}$
G-M	$G=\frac{M}{2M-1}$	$G=\frac{M}{2M-1}$	$G=\frac{M}{2M^2-1}$	$G=\frac{M^2}{2M-1}$
V_s/V_{dc}	$2-\frac{1}{G}$	$2-\frac{1}{G}$	$\frac{\sqrt{8G^2+1}-2-8G^2}{\sqrt{8G^2+1}}$	$\frac{2G-1}{G}\frac{G}{2G-1}$
V_{L2}/V_{dc}	1	$2-\frac{1}{G}$	$\frac{1+\sqrt{1+8G^2}}{4G}$	$\frac{1}{2}2-\frac{1}{G}$
V_{c34}/V_{dc}	NA	NA	1	$1-\frac{1}{2G}$

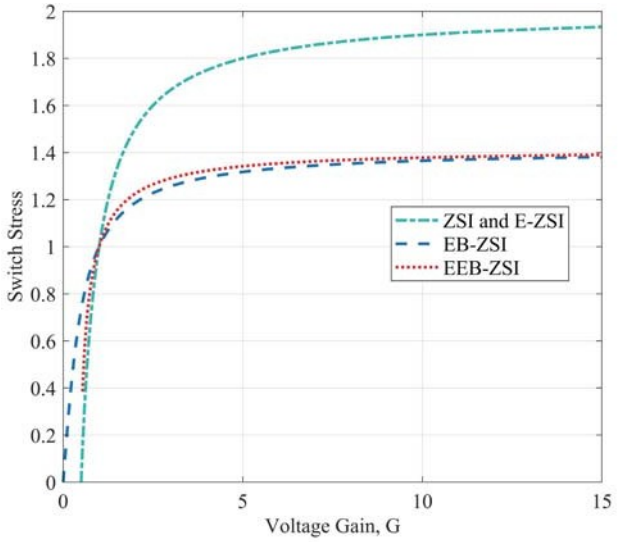

Fig. 10: Comparison of switch stresses.

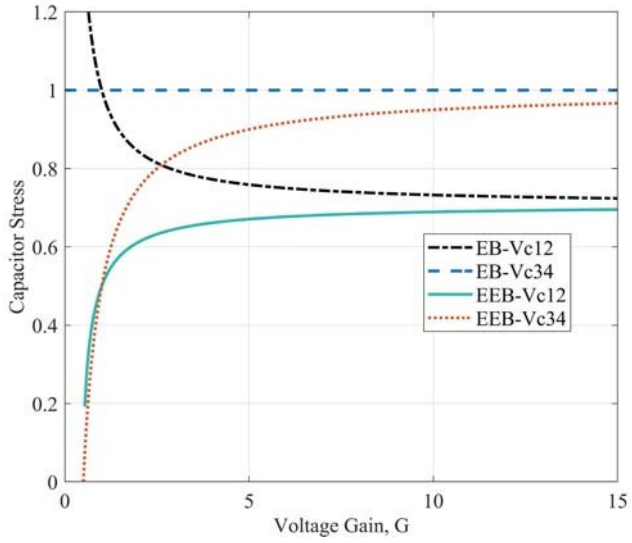

Fig. 11: Capacitor voltage stress comparison of the EB-ZSI and the proposed EEB-ZSI

the same voltage gain. It is thus confirmed that the superior performance of the proposed topology over the EB-ZSI has been achieved.

Table: 2
EEB-ZSI PARAMETERS

Parameter	Symbol	Value
dc input voltage	*Vin*	100 *V*
EEB-ZSI inductance	*L*	650 μH
EEB-ZSI capacitor	*C*	60 μF
Load inductance	R_f	3 *mH*
Load resistance	L_f	40 Ω
Switching frequency	*fs*	5 *kHz*

IV. SIMULATIONS AND EXPERIMENTALTESTS

In order to validate the proposed EEB-ZSI topology, simulations and experimental tests are performed. System parameters are shown in Table II for both simulation and experimental cases.

A. Simulation Results:

The proposed topology is simulated in the PLECS and MATLAB/Simu link with an open-loop control. The simu- lation results are shown in Fig. 12, where M = 0.775, D = 0.225, and V_{dc} = 40 V. According to (15), the boost factor can be calculated as B = 3.85, and thus, the dc-link voltage should be boosted to 154 V (the peak). From the simulation results, it is obvious that the capacitor voltages of V_C1, V_C2, V_C3, $V_C4$are, boosted to 77 V (V_C1=V_C2) and 99 V (V_C3=V_C4), respectively, and the peak dc-link voltage V_{dc} is boosted to 154 V, as expected. Additionally, all the inductor currents increase when the dc-link voltage remains zero during the shoot-through state, as shown in Fig. 12(b). This means that the DC currents are continuous. In order to compare the capacitor stress between the EZ-ZSI and EEB-ZSI, another simulation is carried out and the results show that the capacitor stress of the EZ-ZSI is higher than the proposed EEB-ZSI to achieve the same voltage gain, as indicated in Fig. 12(c). This is in agreement with the theoretical analysis.

B. Experimental Results:

An experimental setup is built up in the lab to ver- ify the performance of the proposed topology. The entire system is controlled by a digital signal processor (DSP) TMS320F28335. The experimental results are shown in Fig.

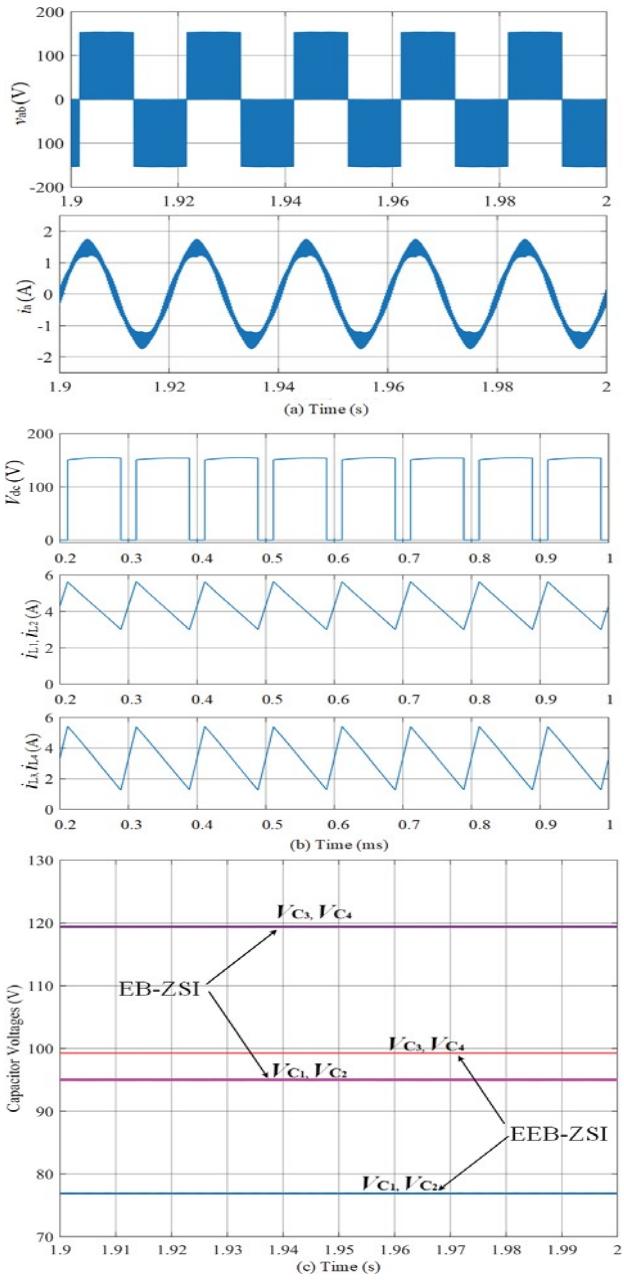

Fig. 12: Simulation results of the proposed Embedded Enhanced-Boost Z- source Inverter (EEB-ZSI), (a) the output leg voltage and load current in EEB-ZSI, (b) the dc-link voltage and inductor currents in EEB-ZSI, and (c) the voltages of the capacitors in the EZ-ZSI and the EEB-ZSI.

The capacitor voltages V_C1, V_C2, and V_C3, V_C4 are, boosted to 73 V (V_C1=V_C2) and 92 V (V_C3=V_C4), and the peak dc-link voltage V_{dc} is boosted from 40V to 148V, as

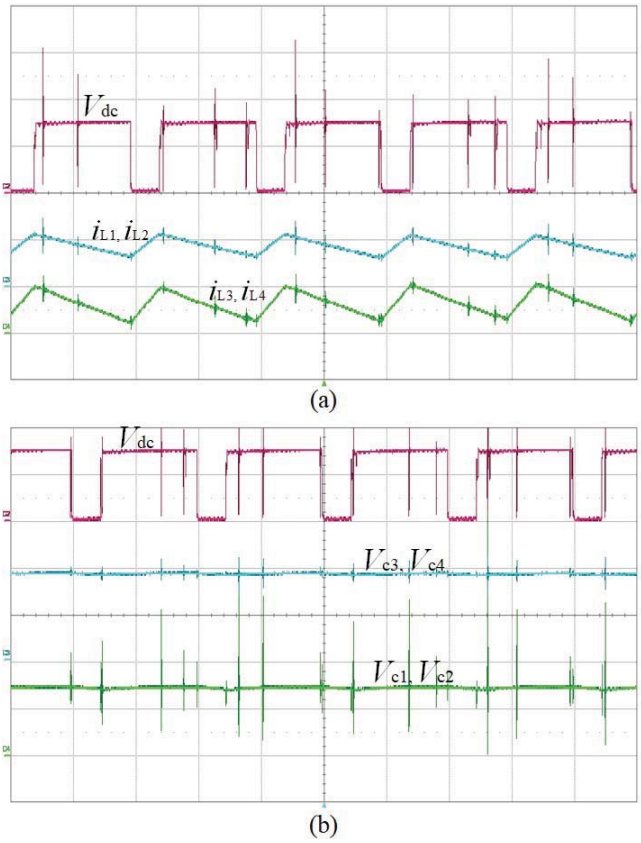

Fig. 13: Experimental results of a three-phase EEB-ZSI system, (a) the dc- link voltage V_{dc} [100 V/div] and inductor currents i_L1, i_L2, i_L3, i_L4 [5 A/div], (b) the dc-link voltage V_{dc} [100 V/div] and capacitor voltages V_C1, V_C2, V_C3, V_C4 [50 V/div].

shown in Fig. 13(a). Compared with simulation results, the boost factor of the experimental results is slightly low due to the effect of the parasitic components in the inductors and capacitors. Moreover, the dc source currents in Fig. 13(a) are continuous. Notably, there are voltage spikes appearing in the dc-link voltage, as shown in Fig. 13. This is possibly due to the electromagnetic interference, which should be improved further.

V. CONCLUSION

In this paper, an Embedded Enhanced-Boost Z-source Inverter (EEB-ZSI) was proposed. Compared with the Enhanced-Boost ZSI (EB-ZSI), the current from the dc source in the proposed topology is continuous. Two dc sources are embedded into the symmetrical Z-source net- works in the proposed topology. Additionally, the capacitor voltage stress of the proposed EEB-ZSI topology is lower than the EB-ZSI due to the embedded configuration. Simulation and experimental results have demonstrated that the proposed topology has a similar boost capability as the EB- ZSI and better performance than the EB-ZSI in terms of voltage stresses of capacitors.

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