Design and Analysis of Low Power Wallace Tree Multiplier

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Abstract -- In this project, a new binary counter design is proposed. It uses 3-bit stacking circuits, which group all of the "1" bits together, followed by a novel symmetric method to combine pairs of 3-bit stacks into 6-bit stacks. The bit stacks are then converted to binary counts, producing 6:3 counter circuits with no XOR gates on the critical path. This avoidance of XOR gates results in faster designs with efficient power and area utilization. In VLSI simulations, the proposed counters are 30% faster than existing parallel counters and also consume less power than other higher order counters. Using the new counter design Wallace tree multiplier was produced. Wallace tree multiplier will be designed of multiplication of n-bits should be used .Based on that the Wallace tree multiplier architecture has been proposed. The proposed multiplier utilized the maximum combinational path delay of 27.711ns. This multiplier has also been designed by using cadence tool to view the less number of transistors usage. In turn the minimum power was required

Indexed terms - counter, stacks, Wallace tree multiplier.

I.INTRODUCTION

Wallace tree multipliers are used to reduced the number of stages required for bit multiplication. And also it will be easy way of multiplication to be implemented in such a way of it will be used. A new counter will be used for the reduction of the stages to be required. Counter will be designed for the reduction of the partial products to be generated. The binary multiplication of integers or axed-point numbers results in partial products that must be added to produce the anal product. The addition of these partial products dominates the latency and power consumption of the multiplier. In order to combine the partial products efficiently, column com- press ion is commonly used. The addition of these partial products dominates the latency and power consumption of the multiplier. In order to combine the partial products efficiently, column com- press ion is commonly used. Through several layers of reduction, the number of summands is reduced to two, which are then added using a conventional circuit. To achieve higher efficiency, larger numbers of bits of equal weight can be considered. The basic method when dealing with larger numbers of bits is the same: bits in one column are counted, producing fewer bits of different weights. The 6:3 counter circuits can be constructed using full and half adders. VLSI simulation results show that our 6:3 counter is at least 30% faster than existing counter designs while also using less power. Simulations were also run on full multiplier circuits for various sizes. Use of the proposed counter improves multiplier efficiency for larger circuits, yielding 64- and 128-bitmultipliers that are both faster and consume less power than other counter based Wallace (CBW) designs.

II WALLACE TREE MULTIPLIER

A Wallace tree multiplier is a multiplier used for the faster than other multiplier circuits to be used in the normal days. This multiplier is used for larger multiplication of the bits. So that of larger multiplication bits lot of partial products to be produced. So that of larger partial products a new counter to be designed in that specification of 6:3 counter as well as 7:3 counter.

A Wallace tree has three steps:

1. Applying a full adder to each column that contains three bits.
2. Applying a half adder to each column that contains two bits.
3. Passing any single bit columns to the next stage without processing.

This reduction method is applied to each successive stage until only two rows remain. This process is illustrated by the conventional 8- bit by 8-bit Wallace multiplier as shown in fig.1.The reduction is performed in four stages. The third phase will require

a wide adder, where s-number of stages in reduction [3].The reduction stage of the Wallace tree multiplier is done by grouping the partial product as full adder and half adder. A Multiplier consists of various stages of full adders, each higher stage adds up to the total delay of the system. In the first and second stages of the Wallace structure the partial product does not depend upon any other values other than the inputs obtained from the AND array [3]. However, for the immediate higher stages, the final value (PP3) depends on the carry out value of previous stage. This operation is repeated for the consecutive stages. Hence, the major cause of the delay is the propagation of the carry out from the previous stage to the next stage. The operation of the Wallace tree multiplier is divided in three steps as

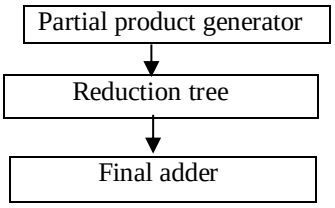

Fig1.Steps of Wallace tree multiplier

III.EXISTING SYSTEM

A. Counter:

Normally counters are designed using the adder circuits like full adders and half adders. Before of the new counter design using of stacker circuits, this type of proposed method will be used for long time, now the new invention of new counter designs, and the usage of this counter slowly down in descending manner. To achieve the higher efficiency, larger number of bits of equal weight can be considered. The basic method when dealing with larger number of bits in the same, bits in one column is counted producing fewer bits of different weights. So that usage only of adder circuits this will contains more the number of gates which will leads to the propagation delay. And this type of counter are used in multiplier circuits like Wallace tree multiplier. In the Wallace tree multipliers after the generation of partial products using these counters leads to take more amount of time as well as more stages to be required for the getting results. And the more number of gates in the circuit so there will be the more number of XOR gates in critical path there will leads to delay. Because of more number of gates there will be the more power consumption. The architecture of 6:3 counter using the full adders and half adder are adders circuits will be below

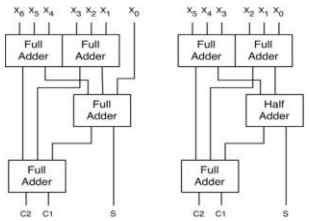

Fig .2 Counter (6:3 and 7:3) using full adders and half adders

In this 6:3 counter consists of full adders and half adders in multiple numbers. x0,x1,x2,x3,x4,x5 are the inputs to be set by users and produced outputs will be s,c1,c2.Inputs will be chosen by users and the counter used to producing outputs. And also in the :3 counter consists of full adders and half adders in multiple numbers,like that the 6:3 counter design x0,x1,x2,x3,x4,x5 ,x6 are considered as the inputs for the 7:3 counter. And also the output for the 7:3 counter like that the 6:3 counter s, c2, and c1 are outputs.

B. Wallace Tree Multiplier:

Wallace tree multiplier has the following steps to be followed by multiplier.

They are

1) Partial product generator
2) Reduction tree
3) Final adder

A5 a4 a3 a2 a1 a0
B5 b4 b3 b2 b1 b0

C5 c4 c3 c2 c1 c0
D5 d4 d3 d2 d1 d0
E5 e4 e3 e2 e1 e0
F5 f4 f3 f2 f1 f0
G5 g4 g3 g2 g1 g0
H5 h4 h3 h2 h1 h0

S8 s7 s6 s5 s4 s3 s2 s1 s0
C6 c5 c4 c3 c2 c1 c0
S14 s13 s12 s11 s10 s9 s8
C10 c9 c8 c7

S14 s20 s19 s18 s17 s16 s1 s0
C16 c15 c14 c13 c12 c11
C10 c9 c8 c7

S26 s25 s24 s23 s22 21 s15 s1 s0
C21 c20 c19 c18 c17

X13 x12 x11 x10 x9 x8 x7 x6 x5 x4 x3 x2 x1

Fig.3 working of Wallace tree multiplier using full adders and half adders

The function of the Wallace tree multiplier only using the full adders and half adders with the explanation is give below with the suitable example:

For the 6_bit Wallace tree multiplier
The given inputs are
a0,a1,a2,a3,a4,a5 and b0,b1,b2,b3,b4,b5

And the resultant outputs are
Z0,z1,z2,z3,z4,z5,z6,z7,z8,z9,z10,z11,z2,z13

For the 8-bit Wallace tree multiplier
The given inputs are
A0,a1,a2,a3,a4,a5,a6,a7 and b0,b1,b2,b3,b4,b5,b6,b7

And the resultant outputs are
Z0,z1,z2,z3,z4,z5,z6,z7,z8,z9,z10,z11,z12,z13,z14,z15,z16,z17.

IV.PROPOSED SYSTEM

7:3 Counter:
The proposed 7:3 counter based on bit stacking has no XOR gates on its critical path, it operates nearly 30% faster than all other counter designs. Thus, this novel method of counting via bit stacking allows construction of a counter for a substantial performance increase without increasing power consumption. 6:3 counter implementations in terms of latency, average power consumption, and number of transistors used. Average power consumption was calculated by integrating the spectra instantaneous power consumption out- put and dividing by the simulation runtime. For the proposed counter, these results are for the entire counter including the 3-bit-stacker circuits and binary conversion logic. The counter based wallace tree multiplier design was used for each simulation, while the internal counter was verified. Use of the proposed counter improves multiplier efficiency for larger circuits, yielding 64 and 128 bit multipliers that are both faster and consume less power than other counter based Wallace(CBW)designs .The proposed 7:3 counter using the symmetric stacker is given below with input and output.

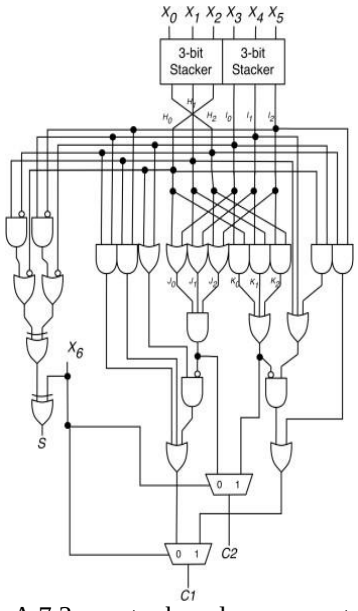

Fig 4. A 7:3 counter based on symmetric stacking

6:3 Counter:
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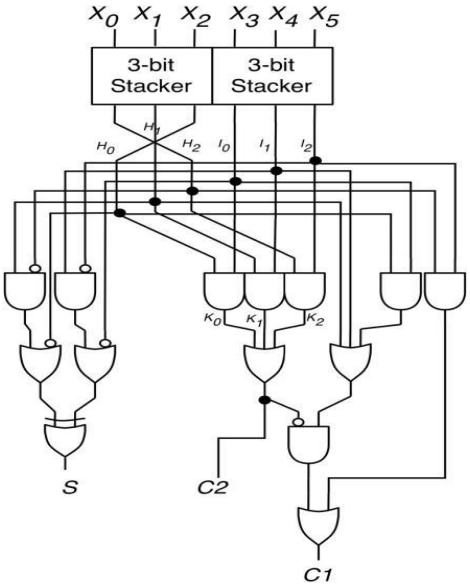

Fig.5. A 6:3 counter based on symmetric stacking

This proposed 6:3 counter will be designed of 3 bit stacker and also with the normal gates. And there is no delay because of the no XOR gates in the critical path. Because of low less amount of delay in this proposed method.

3-Bit Stacking Circuit:
Given inputs X0, X1, andX2, a 3-bit stacker circuit will have three outputs Y0, Y1, andY2 such that the number of "1" bits in the outputs is the same as the number of "1" bits in the inputs, but the "1" bits are grouped together to the left followed by the "0" bits.

It is clear that the outputs are then formed by

$$Y0 = X0 + X1 + X2$$
$$Y1 = X0X1 + X0X2 + X1X2$$
$$Y2 = X0X1X2.$$

Namely, the first output will be "1" if any of the inputs is one, the second output will be "1" if any two of the inputs are one, and the last output will be one if all three of the inputs are "1."The Y1 output is a majority function and can be implemented using one complex CMOS gate.

The 3-bit stacking circuit is shown in below

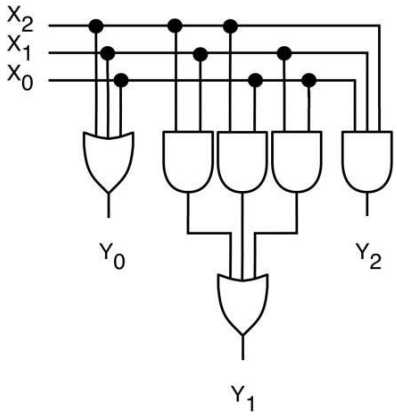

Fig.6.Three –bit stacker circuit

This paper presents a counting method that uses bit stacking circuits followed by a novel method of combining two small stacks to form larger stacks. Additionally, counter designs as in and use multiplexers to reduce the number of XOR gateson the critical path. Some of these muxes can be implemented with transmission gate logic to produce even faster designs. To form a 6-bit stacking circuit using the 3-bit stacking circuits discussed. Given six inputs X0... X5, we first divide them into two groups of 3 bits which are stacked using 3-bit stacking circuits. Let X0, X1, and X2 be stacked into signals named H0, H1, and H2 and X3, X4, andX5 be stacked into I0, I, and I2. First, we reverse the outputs of the first stacker and consider the six bits H2, H1, H0, I0, I1, and I2. See the top of Fig. given below for an example of this process. We notice that within these six bits, there is a train of "1" bits surrounded by "0" bits. To form a proper stack, this train of "1"bits must start from the leftmost bit. In order to form the proper 6-bit stack, two more 3-bit vectors of bits are formed called J0, J1, J2 and K0, K1, K2. The idea is to fill the J vector with one's first, before filling the K vector.

Wallace Tree Multiplier:
A proposed Wallace tree multiplier was designed for reduction of partial products to be generated in the multiplication of bits. Reduction of bits can be made of counter circuits like 6:3 counter and also 7:3 counter designed was already described. If the inputs are in the numbers of 7 bits had the getting outputs will be the number of 3 bits. This is easy to access the bits to be used in counter. So that of the new counter design the number of stage used for reduction of partial products should be reduce din following manner. And also for the reduction of the partial products to be used the full adders and also the half adders.

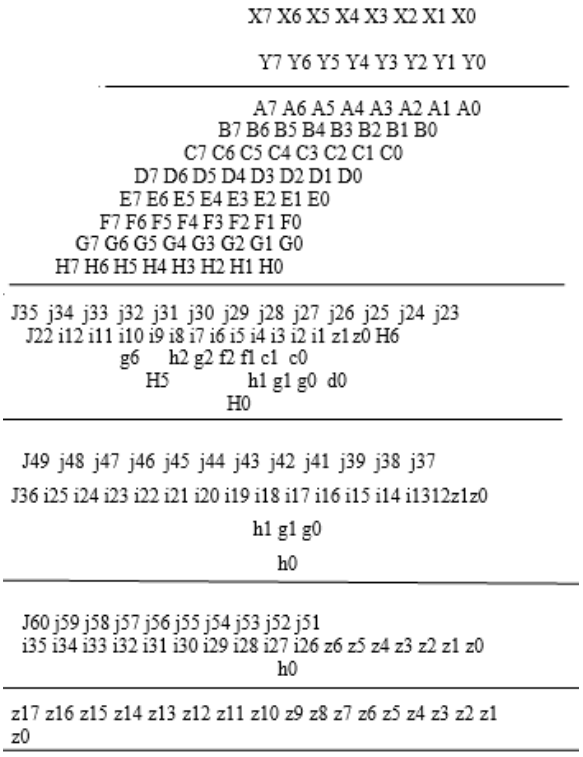

Fig: 7. working of counter based Wallace tree multiplier

The resultant outputs for the ordinary Wallace tree multiplier and also for the counter based Wallace tree multiplier will be the same. But the reduction stages for the partial products will be different. The resultant outputs for the ordinary Wallace tree multiplier and also for the counter based Wallace tree multiplier will be the same. But the reduction stages for the partial products will be different. And also be the because of reduced number of stages will also reduce the number of transistor required for the simulation. While the proposed counter is still slightly faster than the existing counters, the improvement is not as significant and the power consumption is increased. For this reason, we will use the proposed 6:3 counter to build 64-bit multipliers.

V.RESULT AND DISCUSSION

Simulation output for 8 bit Wallace tree multiplier:

Simulation was performed using the Xilinx tool for the 8-bit Wallace tree multiplier for the some set of input and getting the resultant outputs

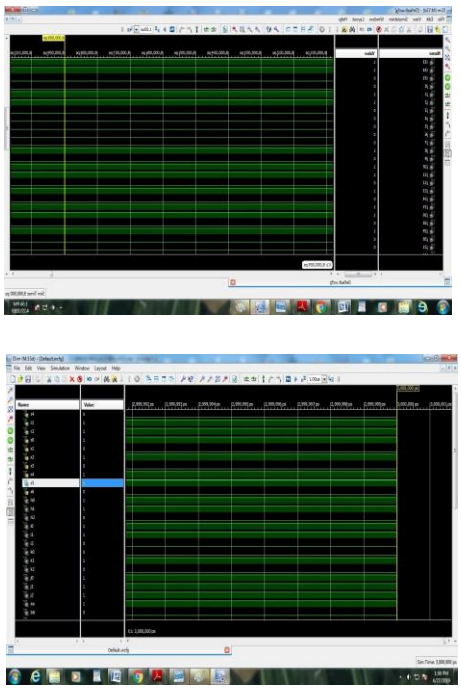

Fig.8 Simulation of 6.3 counter:

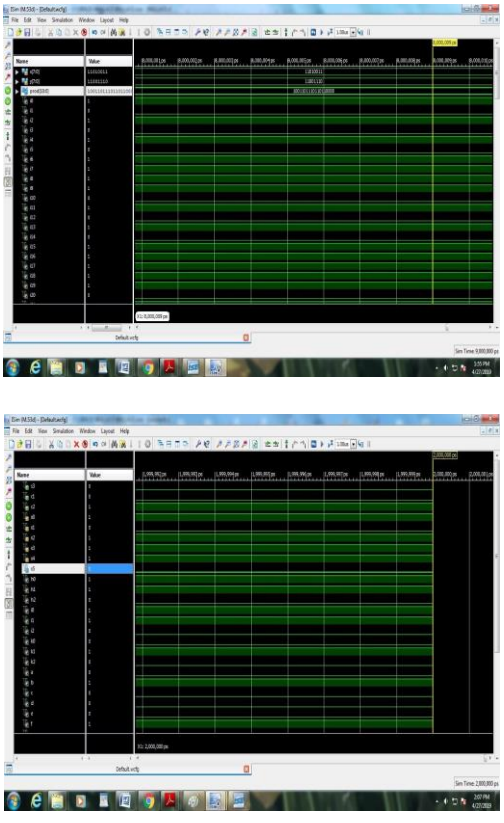

Fig.9 Simulation of 6.3 counter:

VI.CONCLUSION

In this brief, a new binary counter based on novel symmetric bit stacking approach is proposed. The Wallace tree multiplier has been designed using the 6:3 counter as well as 7:3 counter.This method shown that counting method can be used to implement 6:3 and 7:3 counters, which can be used in any binary multiplier circuit to add the partial products. This has been demonstrated that 6:3 counters implemented with this bit stacking technique to achieve higher speed than other higher order counter designs while reducing power consumption. This is due to the lack of XOR gates and multiplexers on the critical path. The 64-bit and 128-bit counter- based Wallace tree multipliers built using 6.3 counter and 7.3 counter.

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