Cascaded H Bridge 17 Level Inverter with PWM Technique

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Abstract- ***A Multilevel inverter is a very important tool for PV Array and Electric Vehicle etc. in Modern ERA Because the non-renewable energy is important for our future. The non-renewable energy is reducing the pollution and carbon content in the environment and also reducing the fossil fuel requirement for transportation and producing electricity. The multilevel inverter can provide higher level of sinusoidal output with less total harmonic distortion with the help of pulse width modulation. Different type of Pulse width modulation like POD APOD etc. can be implemented. 17 level inverters with the use of Phase Opposition Disposition pulse width modulation (POD-PWM) technique with 16 carrier signals with cascaded inverter with 16 IGBT switches is proposed. All the carrier signals are above X-axis are out of phase with the below signal by 180º. Total harmonic distortion of load voltage is 7.26% and load current is 3.09% obtained. This inverter can be use with solar photo voltaic cell. By the use of this inverter the higher-level output and less harmonic distortion output obtained. By the use of this output the electrical equipment is in very safe condition.***

Indexed Terms- ***Multilevel inverter, PWM, POD, Total Harmonic distortion,***

I. INTRODUCTION

The technique for the half-bridge inverter is optimized subjected to the constraint of switching frequency of the SCR's, used the concepts of modern control theory. Variable-frequency variable voltage sinusoidal output in three phase inverters was possible by employing the techniques developed in [1] new neutral-point-clamped pulse width modulation (PWM) inverter composed of main switching device which operated as switches for PWM and auxiliary switching devices to clamped the output terminal potential to neutral point potential had been developed in [2] A new commutation circuit, especially suitable for pulse width-modulated (PWM) inverters, was described. The circuit did not require recharging of a commutation capacitor and was therefore ready for commutation at any time and this improved the Circuit efficiency in [3] a generalization of the PWM "subharmonic" method to control single phase or three phase multilevel voltage source inverters (VSI) is revel in the [4-8] Multilevel Inverter was a key technology and plays critical role in AC motor drives, uninterruptible power supplies, high-voltage DC power transmission, flexible AC transmission systems, static var compensators, active filters, electric and hybrid electric vehicles and integration and utilisation of renewable energy sources [9,10]. In the field of high-power medium voltage DC/AC conversion, MLI is getting tremendous popularity together in terms of topology & control scheme because of its decent power quality, less total harmonic distortion (THD), reduced voltage tension across the switches, good electromagnetic compatibility, fewer switching losses and dv/dt stress. However, MLI possess some disadvantages, that was, to rise output levels, the number of semiconductor switch necessity along with peripherals devices like gate driver circuit, protection circuit & heat sink rises. Increased device count makes overall system complex, bulky & costly and reduced the efficiency and reliability of the converter.

Traditionally, MLIs are classified as cascaded H bridge (CHB), flying capacitor (FC) & neutral point clamped (NPC). In past few decades, most of the literatures printed showed the study on CHB, FC and NPC topologies with respect to their corresponding advantages and disadvantages [10] A CHB MLI was composed of several H bridge cell & isolated DC source. On the basis of voltage magnitude DC source, CHB was classified as asymmetric and symmetric configuration. In symmetric configuration, magnitudes of DC sources were equal (V1 = V2 = V3…), whereas in asymmetric configuration

magnitudes of DC sources were not equal (V1 ≠ V2 ≠ V3….). The asymmetric configuration of CHB produces higher number of voltage level as equated with symmetric configuration for same number of power switches [10] Along with investigation of CHB, researchers paid dedicated effort & attention to develop newer application-oriented topologies with concentrated number of device count & complexity. Consequently, in past few years, big numbers of control scheme and topologies had been projected with reduced device count which utilizes combination of unidirectional and bidirectional switches of different ratings [10] some of them were reviewed here briefly.in [13-17] symmetrical topologies of MLIs were discussed, the cost of these inverters was less because of small variety of DC sources, but modularity of those MLIs is foremost concern in several applications. Similarly, in [8] asymmetrical topologies of MLI through condensed number of switches were presented, but the necessity of great number of bidirectional switches is a main issue in these topologies. In [9] different type of topology such as hybrid bridge module, full bridge module, DC MLI Cascaded etc. were focused. From different type of topology H-bridge multilevel pulse width modulation converter topology based on a series connection of a high-voltage diode-clamped inverter and a low-voltage conventional inverter reveal in [10] The Neutral Point Inverter was used with diode and transistor which called as diode bypassed neutral point converter for that configuration, each dc source contributes only to one half-cycle of the output waveform, either positive or negative was required. In that configuration the drawback was losses for a diode bypassed configuration are expected to be greater than for the full transistor configuration [15] another topology which was cascade switched-diode multilevel converter which can harvest several levels with minimum number of power electronic switches, gate driver circuits, power diodes, & dc voltage sources. The number of essential power electronic switches against essential voltage levels was a very significant factor in designing of multilevel converter, as switches define the reliability, circuit size, cost, installation area, and control complexity. For asymmetric and cascade converter, new algorithms for determination of dc voltage sources values were presented. To harvest extreme number of levels at the output voltage, the planned cascade topology is optimized for distinct goals, such as minimization of number of power electronic switches, gate driver circuits, power diodes, dc voltage sources, & blocking voltage on switches. Comparison of the outcomes of various multilevel converters will be inspected to reflect the advantages of the existing topologies [17]. In this paper, new topology of symmetrical MLI is proposed which used hexagon switch cell (HSC). The proposed topology was capable of making 7-/9-/11-output levels by employing 7 controlled switches. It had modular structure & offers reliable process with reduced voltage pressure across the switches. inherent harmonizing of capacitor voltage minimized diversity of DC source. The symmetrical arrangement of proposed topology creates higher number of output levels through relatively a smaller number of switches. numbers of bidirectional switches also diminish considerably in the proposed topology. An in-depth comparison of proposed topology with standard topologies & most recent work in field is carried out to highlight the benefit and novelty of the planned topology. The cascade technology enhances output of the inverter and Total harmonic distortion of the inverter this topology was given by [21-24] so that 9 level inverters also elaborated on that paper for less harmonics output.

II. MLI TOPOLOGY

2.1 Topology-I

The configuration of topology-I is illustrated in Fig. 1a. It comprises of two DC voltage source VS1 and VS2, along with capacitor C1 & C2 which forms voltage divider circuit. An auxiliary switch is designed by controlled switch four diodes D7, D8, D9, D10 and S7 which are connected to HSC collected by six switches S1, S2, S3, S4, S5 and S6. When the values of the DC voltage sources are equal, that is, VS1 = VS2 then it can be referred to as symmetrical MLI otherwise asymmetrical. Topology-I is proficient of making 7-/9-/11-level output with certain grouping of DC voltage source while integrating only seven-controlled switches.

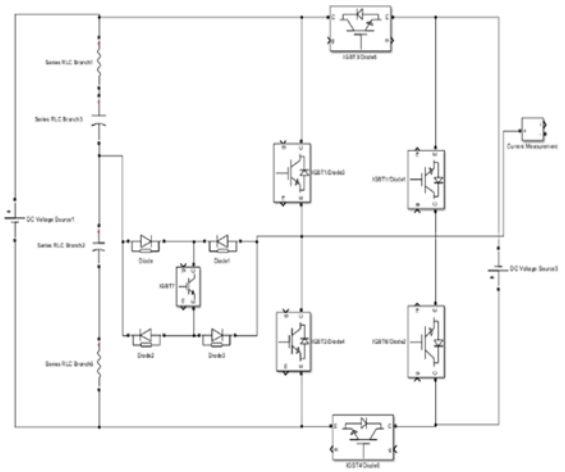


Fig.1 H Bridge Level Topology

III. PROPOSED MLI TOPOLOGY

3.1 Proposed topology-II, that is, proposed cascade connected MLI

A MLI synthesizes a stepped waveform containing of input DC levels & their additive and/or subtractive groupings. Thus, voltage waveform comprises of multiple 'levels' with both 'positive' & 'negative' polarities (in positive and negative half cycles, respectively). Many a times, a MLI topology synthesizes the multiple stages with only one polarity & H bridge was used as polarity converter as offered in [18] These parts were, respectively, referred as 'polarity-generation part' and 'level-generation part'. It was significant to mention here that power switches for the polarity generation part essential to have a lowest voltage rating equal to the operating voltage of the MLI. Hence, in the topologies presented in [15-17] the H-bridge was used as polarity generator & the switches of H bridge must be able tolerate voltage equal to rated output voltage of MLI. These 4 switches of H bridge turn 'ON' and 'OFF' once throughout a fundamental cycle, hence these 4 switches restrict the application of offered topologies for high voltage.

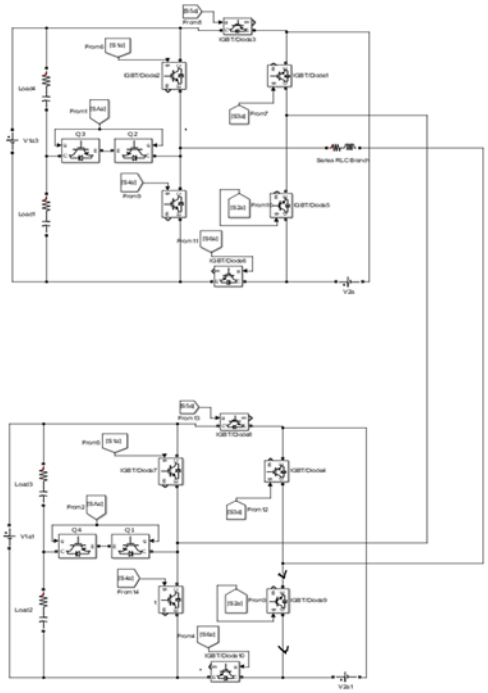
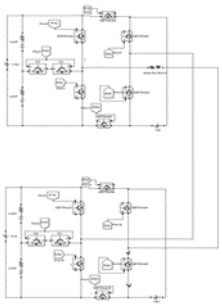


Fig.2. Cascaded Topology of H Bridge

when compared with 4 of those topologies accessible in [15-18]. These 2 switches are low frequency high voltage switches which are turned 'ON' & 'OFF' once during a fundamental cycle, hence conduction and switching losses decreases by considerable amount. Still problem perseveres with the 2 switches, that is, S3 and S4 have to bear full rated voltage which counterattacks application of planned topology-I in advanced voltage applications. Hence, in order to overcome this problematic cascade connection of proposed topology-I is used which is shown in Fig. 3. The arrangement of proposed topology-II is shown in Fig. 3. It is change of topology-I in order to overawed the problem of voltage stress across the switches so that proposed topology can be functional in higher voltage application. Topology-II is also self-possessed of one auxiliary switch connected to HSC. composed switch network is supplied by 2 DC voltage source sideways with 2 capacitors. It comprises cascade connection of numerous fundamental cells that can be functioned for higher voltage applications in symmetrical configuration. Each cell contains 7 controlled switches, 10 power diodes, 2 DC sources & two capacitors. The DC source on individually cell is numbered as VS1,1, VS2,1, ..., VS1, n, VS2,n ('where n denotes number of cascaded cell'). different operating modes & switching states along through

corresponding output voltage levels for 17-level inverter are summarized in Fig. 4. The generalization of topology-II in symmetrical configuration for N-level output is given as Total number of controlled switches required = 7 8 × (N − 1) (5) Total number of diodes required = 5 4 × (N − 1) (6) Total number of DC sources required = 1 4 × (N − 1) (7) Total number of capacitors required = 1 4 × (N − 1) (8)



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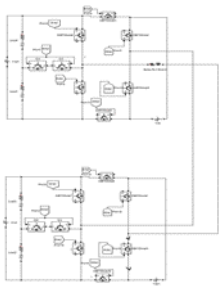

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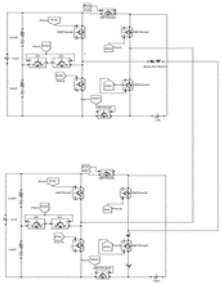

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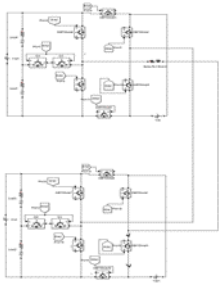

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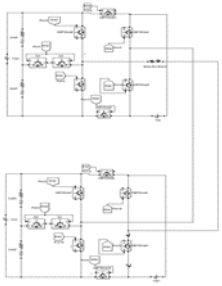

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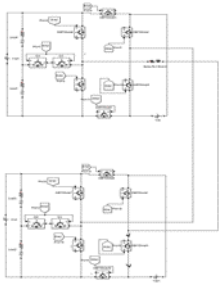

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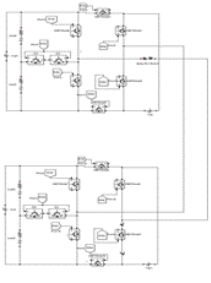

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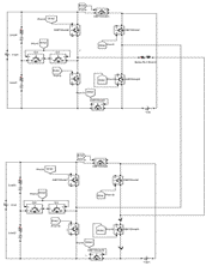

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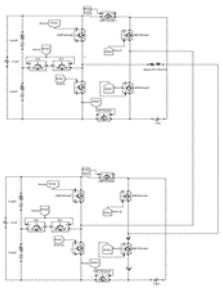

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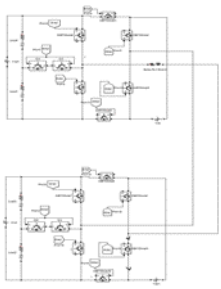

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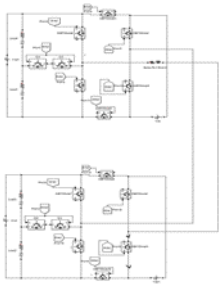

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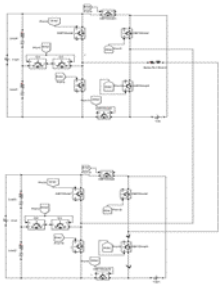

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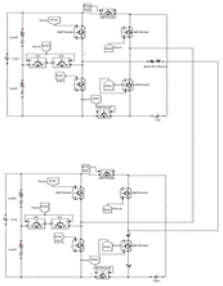

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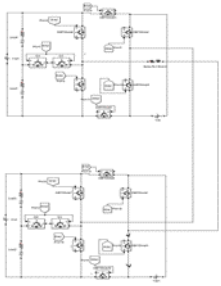

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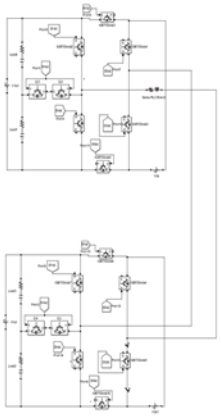

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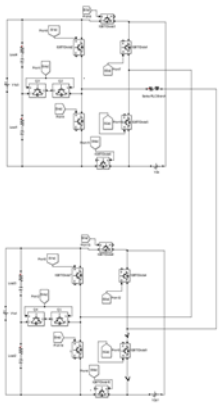

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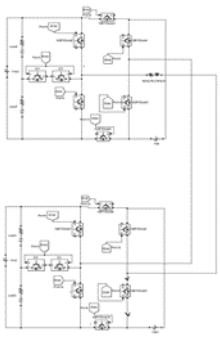


LEVEL 17

Fig.3 Different Level of Multilevel Inverter

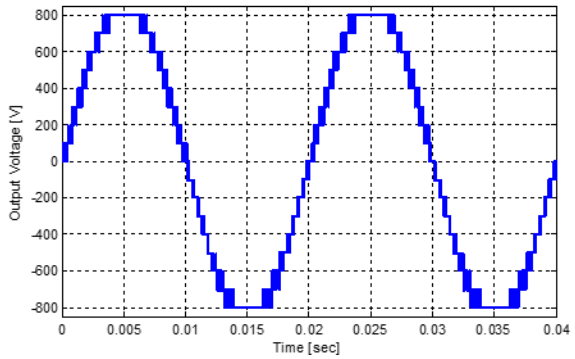
Table 3 Different switching states of topology-I for seventeen-level output.

Levels	ON state Switches
1	S1a, S3a, S6a, S1b, S3b, S6b
2	S1a, S3a, S6a, SAB, S3b, S6b
3	S1a, S3a, S6a, S3b, S4b, S6b
4	S1a, S3a.S6a. SAb, S2b, S6b
5	S1a, S3a
6	SAa, S3a, S5a, S2b, S4b, S6b
7	S3a,S4a,S6a,S2b,S4b,S6b
8	SAa, S2a, S6a, S2b, S4b, S6b
0	S2a, S4a, S6a, S2b, S4b, S6b
1	SAa, S3a, S5a, S1b, S3b, S5b
2	S1a, S2a, S5a, S1b, S3b, S5b
3	SAa, S2a, S5a, S1b, S3b, S5b
4	S2a, S4a, S5a, S1b, S3b, S5b
5	S2a, S4a, S5a, SAb, S3b, S5b
6	S2a, S4a, S5a, S1b, S2b, S5b
7	S2a, S4a, S5a, Sab, S2b, S5b
8	S2a, S4a, S5a, S2b, S4b, S5b

Parameters	Cascade Topology
Source -1	Vs1,1=200, Vs1,2=200
Source -2	Vs2,1=200, Vs2,2=200
capacitor, µF	1200
R, Ω	50
Switching frequency HZ	100
Modulation index	Unity

IV. SIMULATION AND EXPERIMENTAL RESULTS

Modulation scheme multi-carrier pulse width modulation technique has been working with carrier frequency of 100 and 5000 Hz, where reference signal frequency is kept at 50 Hz. In multi carrier pulse width modulation scheme, carrier signals are related with reference signal & pulses so obtained are used for switching of devices consistent to their respective voltage levels. Number of carriers rises as the number of levels rises and the raise is directly proportional



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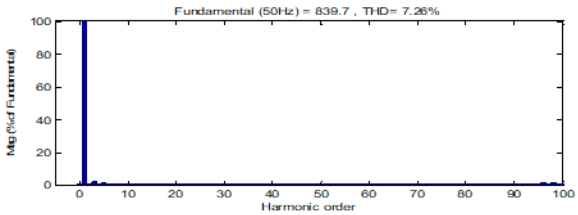
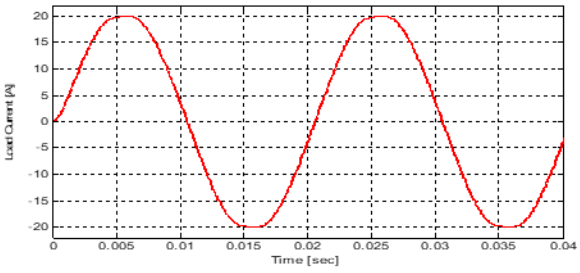


(b)

Fig.4 (a) Seventeen-level output voltage of the proposed MLI, (b) Corresponding THD



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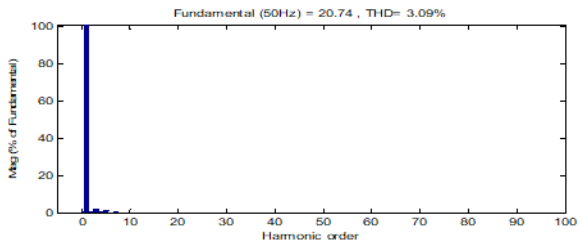

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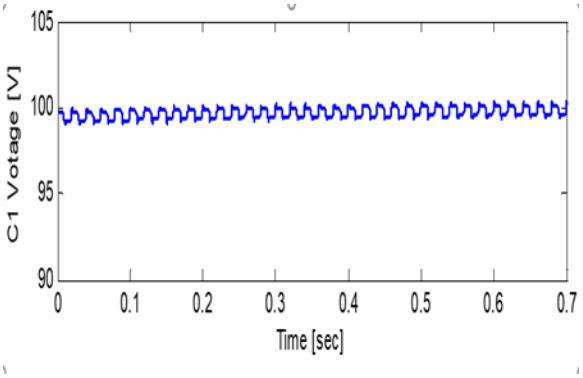
Fig.5 (a) Load current of the proposed MLI, (b) corresponding THD



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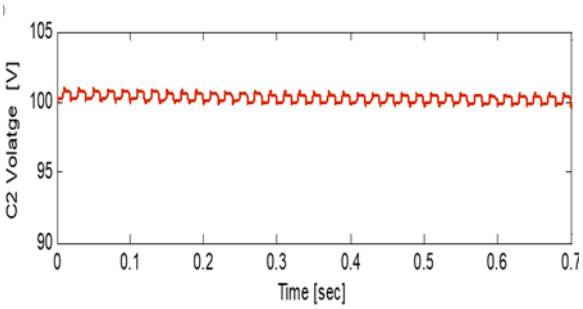

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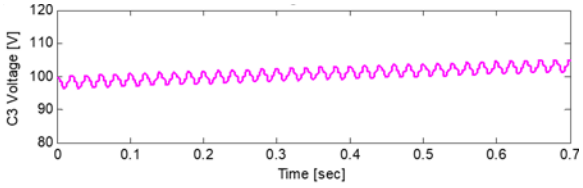
Fig.6 (a) Capacitor (C_1) Voltage (b) Capacitor (C_2) Voltage



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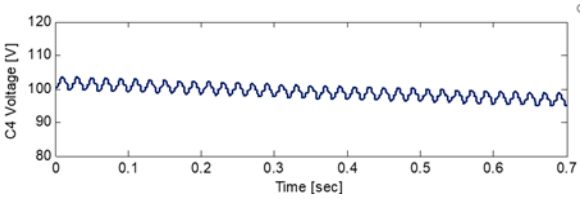

(b)

Fig.7 (a) Capacitor (C_3) voltage (b) Capacitor (C_4) voltage

CONCLUSION

The H Bridge cascade topology Multilevel inverter is switched with Pulse width modulation Phase opposition disposition *Technique total harmonic distortion of voltage is 7.26% is obtained and the H bridge topology can be use for 7-9-11-13-17 level inverters, total harmonics distortion is less comparing to the other technology. total harmonic distortion can be reduced with a greater number of cascaded inverters.*

REFERENCES

[1] Hasukh s PATEL RICHARD G. HOFT "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I1-Voltage Control Techniques" IEEE Transection on industrial applications September/October 1974.

[2] AKIRA NABAE, ISAO TAKAHASHI, HIROFUMI AKAGI "A New Neutral-Point-Clamped PWM Inverter" IEEE Transections on industry applications Volume IA-17 N.5 September/October 1981.

[3] PRADEEP M, V. R. STEFANOVIC, "A Versatile Commutation Circuit for PWM Inverters" IEEE Transections on industry applications Volume IA-18 No.2 March/April 1982.

[4] PRADEEP M, V. R. STEFANOVIC "Generalized Structure of a Multilevel PWM Inverter" IEEE Transections on industry applications Volume IA-19 No.6 November/December 1983.

[5] Giuseppe Carrara, Simone Gardella, Mario Marchesoni, Raffaele Salutari, & Giuseppe Sciutto "A New Multilevel PWM Method: A Theoretical Analysis" IEEE Transections on Power Electronics Vol.7 No.3 July 1992.

[6] Leon M. Tolbert, Thomas G. Habetler, "Novel Multilevel Inverter Carrier-Based PWM Method" IEEE Transections on industry applications Volume 35 No.5 September/October 1999.

[7] Brendan Peter McGrath, Donald Grahame Holmes "Multicarrier PWM Strategies for Multilevel Inverters" IEEE Transections on industrial Electronics Volume 49 No.4 August 2002.

[8] Juan Dixon, Luis Morán "High-Level Multistep Inverter Optimization Using a Minimum Number of Power Transistors" IEEE Transections on industrial Electronics Volume 21 No.2 March 2006.

[9] Zhou Jinghua, Li Zhengxi, "Research on Hybrid Modulation Strategies Based on General Hybrid Topology of Multilevel Inverter" Speedam 2008 978-1-4244-1664-6/08 IEEE

[10] Alireza Nami, Firuz Zare, Arindam Ghosh, Frede Blaabjerg, "A Hybrid Cascade Converter Topology with Series Connected Symmetrical and Asymmetrical Diode Clamped H Bridge Cells" IEEE Transections on Power Electronics Vol.26 No.1 January 2011.

[11] P. Palanivel, S.S. Dash, "Analysis of THD & output voltage performance for cascaded multilevel inverter using carrier PWM techniques" IET Power Electron., 2011, Vol. 4, Iss. 8, pp. 951–958.

[12] K k gupta, S. Jain "Topology for multilevel inverters to attain maximum number of levels from given DC sources" ET Power Electron., 2012, Vol. 5, Iss. 4, pp. 435–446.

[13] Ehsan Najafi, Abdul Halim Mohamed Yatim "Design and Implementation of a New Multilevel Inverter Topology" IEEE Transections on industrial Electronics Volume 59 No.11 November 2012.

[14] Raul Rebinoviece, Dmitry Baimel, Jacek Tomasik, Adrian Zuckerberger "Thirteen-level cascaded H-bridge inverter operated by Generic phase shifted pulse-width modulation" IET Power Electron., 2013, Vol. 6, Iss. 8, pp. 1516–1529

[15] Arif Al judi, Edwin Nowicki "Cascading of diode bypassed transistor-voltage source units in multilevel inverters" IET Power Electron., 2013, Vol. 6, Iss. 3, pp. 554–560

[16] Ali Ajami, Mohammad Reza Jannati Oskuee, Ataollah Mokhberdoran, Alex Van den Bossche "Developed cascaded multilevel inverter topology to minimalize the number of circuit devices & voltage stresses of switches" IET Power Electron., 2014, Vol. 7, Iss. 2, pp. 459–466

[17] Rasoul Shalchi Alishah, Daryoosh Nazarpour, Seyed Hossein Hosseini, Mehran Sabahi "Novel Topologies for Symmetric, Asymmetric, & Cascade Switched Diode Multilevel Converter With Minimum Number of Power Electronic Components" IEEE Transections on industrial Electronics Volume 61 No.10 October 2014

[18] Ebrahim Babaei, Saeed Sheer Mohammad Zadeh Gowgani "Hybrid Multilevel Inverter Using Switched Capacitor Units" IEEE Transections on industrial Electronics Volume 61 No.9 September 2014

[19] Mahrous Ahmed, Ahmed Sheir, Mohamed Orabi "Real-Time Solution and Implementation of Selective Harmonic Elimination of Seven-Level Multilevel Inverter" IEEE Journal of emerging and Selected Topics in Power Electronics, Vol. 5, NO. 4, December 2017

[20] Ahmed Salem, Huynh Van Khang, Kjell G. Robbersmyr "New Multilevel Inverter Topology with Reduced Component Count" ISBN: 978-9-0758-1531-3 - IEEE catalog number: CFP19850-ART

[21] Shivam Prakash Gautam, Lalit Kumar, Shubhrata Gupta "Hybrid topology of symmetrical multilevel inverter using less number of devices" IET Power Electron., 2015, Vol. 8, Iss. 11, pp. 2125–2135

[22] Mahendra B. Ghat, Anshuman Shukla, "A New H-Bridge Hybrid Modular Converter (HBHMC) for HVDC Application: Operating Modes, Control and Voltage Balancing"

[23] MARIF DAULA SIDDIQUE. SAAD MEKHILEF, NORAISYAH MOHAMED SHAH, ADIL SARWAR, ATIF IQBAL, MUDASIR AHMED MEMON "A New Multilevel Inverter Topology With Reduce Switch Count"

[24] PRABHU OMER, BALWINDER SINGH SURJAN "A Review on Reduced Switch Count Multilevel Inverter Topologies" IEEE Access