# H Bridge 3 Level Inverter with Pulse Width Modulation Technique

ROHIT KUMAR OBEROY[1], DR. PADMINI SHARMA[2]
[1, 2] *Chhatrapati Shivaji Institute of Technology Durg*

***Abstract-*** ***A Multilevel inverter is a very important tool for PV Array and Electric Vehicle etc. in Modern ERA Because the non-renewable energy is important for our future. The non-renewable energy is reducing the pollution and carbon content in the environment and also reducing the fossil fuel requirement for transportation and producing electricity. The multilevel inverter can provide higher level of sinusoidal output with less total harmonic distortion with the help of pulse width modulation. Different type of Pulse width modulation like POD APOD etc. can be implemented. 3 level inverters with the use of Phase Opposition Disposition pulse width modulation (POD-PWM) technique with 2 carrier signal with inverter with 4 IGBT switches is proposed. All the carrier signals are above X-axis are out of phase with the below signal by 180º. Total harmonic distortion of load voltage is 35.45 % and load current is 35.51 % obtained. This inverter can be use with solar photo voltaic cell. By the use of this inverter the higher-level output and less harmonic distortion output obtained. By the use of this output the electrical equipment is in very safe condition.***

***Indexed Terms-*** ***Multilevel inverter, Inverter, POD, PWM, Total Harmonic Distortion***

## I. INTRODUCTION

The technique for the half bridge inverter is heightened subjected to the limitation of switching frequency of SCR's, used the perceptions of modern control theory. Variable-frequency variable voltage sinusoidal output in three phase inverters was probable by using the methods developed in [1] new neutral-point-clamped pulse width modulation (PWM) inverter collected of core switching devices which operated as switches for PWM & auxiliary switching devices to clamped the harvest terminal potential to neutral point potential had been developed in [2] A novel commutation circuit, specially appropriate for pulse width-modulated (PWM) inverters, was described. The circuit did not require recharging of a commutation capacitor and was therefore ready for commutation at any time and this improved the Circuit efficiency in [3] a generalization of the PWM "subharmonic" method to control single-phase or three-phase multilevel voltage source inverters (VSI) is revel in the [4-8] Multilevel Inverter is a key technology & acting crucial role in AC motor drives, uninterruptible power supplies, high-voltage DC power transmission, flexible AC transmission systems, static var compensators, active filters, electric and hybrid electric vehicles and integration and utilisation of renewable energy sources [9,10]. In the field of high-power medium voltage DC/AC translation, MLI is reception marvelous popularity together in terms of topology & control scheme because of its upright power quality, fewer total harmonic distortion (THD), condensed voltage pressure across switches, good electromagnetic compatibility, less switching losses & dv/dt stress. However, MLI possess almost drawbacks, that is, to growth output levels, the number of semiconductor switch requirement sideways peripherals devices like gate driver circuit, protection circuit & heat sink increases. Improved device count makes total system composite, bulky & costly & reduces efficiency and the reliability of the converter.

Traditionally, MLIs are classified as cascaded H bridge (CHB), flying capacitor (FC) and neutral point clamped (NPC). In past limited decades, utmost of the literatures published displays study on CHB, FC and NPC topologies with reverence to their corresponding benefit and drawbacks (8) A CHB MLI is collected of several H bridge cell & isolated DC source. On the basis of voltage magnitude DC source, CHB is classified as symmetric and asymmetric configuration. In symmetric configuration, extents of DC sources are like (V1 = V2 = V3…), whereas in asymmetric configuration magnitudes of DC sources are not alike

(V1 ≠ V2 ≠ V3….). The asymmetric configuration of CHB harvests advanced number of voltage level as equated with symmetric configuration for equal number of power switches [8] Along with the exploration of CHB, researchers paid devoted effort & attention to evolve newer application-oriented topologies with condensed number of device count & complexity. Consequently, in past few years, bulky numbers of control scheme and topologies have been planned with condensed device count which utilizes a combination of unidirectional & bidirectional switches of diverse ratings [7] The beginning of the transformer less multilevel inverter topology has fetched forth various pulse width modulation (PWM) schemes as a means to regulates the switching of the active devices in individually of the multiple voltage levels in inverter. An analysis of how standing multilevel carrier-based PWM touches switch employment for the diverse levels of a diode clamped inverter is directed in [8] new topology of modular multilevel inverters, being appropriate in medium & high voltage applications. As related to existing circuits This topology has benefit of high 'levels/components' ratio, growing the output voltage levels without increasing voltage pressure across used switches, structure simplicity, isolation features, & modularity. These merits allow it to fit well in high-reliability medium power applications, which necessitate fast troubleshooting & maintenance flexibility is obtained but the limitation of this topology limitations due to using transformers such as size, noise, and presence of leakage is reveal in [20] new topologies for staircase output voltage generations with a reduced number of switch requirement. The first topology necessitates three dc voltage sources & 10 switches to synthesize 15 levels across load. The extension of the 1st topology as the 2nd topology, which comprises of 4 dc voltage sources & 12 switches to accomplish 25 levels at output. Both topologies, apart from having reduced switch count, exhibit merits in terms of condensed voltage stresses across switches. several experimental results prove the suitability & workability of the planned topology with different type of loading groupings considering the modification of modulation indexes in [21] MLI topologies in current years are appealing advanced outputs levels with condensed number of switches. However, great concession has been finished in terms of modularity, simplicity, number of bidirectional switches, variety of DC source, voltage pressure across switches, reliability & losses. Moreover, use of asymmetrical converters is not actually prolonged, because they are not appropriate for industrial applications because modularity is gone and it has diverse type of semiconductors. Hence, this paper emphases on symmetrical MLI topologies & tries to resolve the problems associated to it. In this paper, new topology of symmetrical MLI is planned which uses hexagon switch cell (HSC). The proposed topology is proficient of creating 7-/9-/11- output levels by applying seven controlled switches.

It has modular structure & offers consistent operation with condensed voltage stress across the switches. inherent balancing of capacitor voltage minimalizes variety of DC source. The symmetrical configuration of projected topology produces higher number of harvest levels with comparatively fewer number of switches. Numbers of bidirectional switches also cut considerably in the planned topology. An in-depth assessment of proposed topology with classical topologies & most recent work in the field is arranged out to acme the novelty & benefit of the proposed topology.

## II. PROPOSED MLI TOPOLOGIES

### 2.1 Proposed topology-I

The configuration of topology I is illustrated in Fig. 1a. It consists of two DC voltage source VS1 and VS2, along with capacitor C1 and C2 which forms voltage divider circuit. An auxiliary switch is designed by controlled switch S7 & four diodes D7, D8, D9 and D10 which are associated to HSC collected by six switches S1 , S2 , S3 , S4 , S5 and S6. When the values of the DC voltage sources are equal, that is, VS1 = VS2 then it can be referred to as symmetrical MLI otherwise asymmetrical. Topology-I is capable of making 7-/9-/11-level output with certain grouping of DC voltage source while integrating only 7 controlled switches. output voltage level with particular grouping of DC voltage source is brief in Table 1. The generalised form of planned topology-I is shown in Fig.1

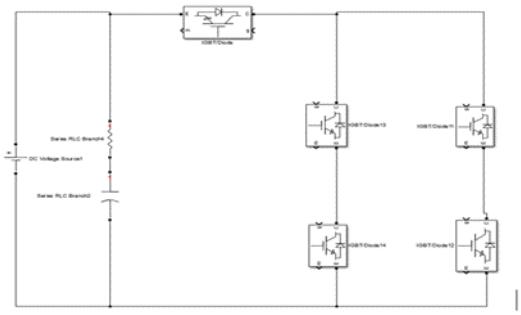
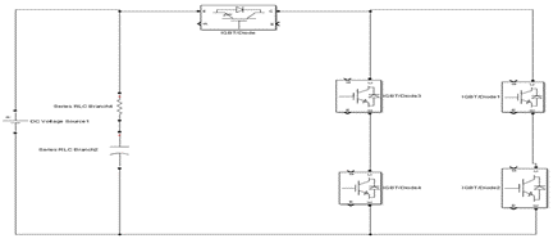


Fig.1 The generalised form of planned topology-I

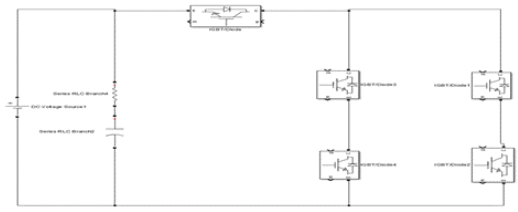
| Algorithm | Values of DC sources | No. of output levels |
|---|---|---|
| First | VS1 | 3 |
| Second | VS1 = 2 × VS2 | 7 |
| Third | VS1 = VS2 | 9 |
| Fourth | VS1 = 2/ 3 × VS2 | 11 |

Table 1 Different combinations of DC voltage source for higher output voltage levels

the table is defined the first position have 3 level having only one voltage source and in the 7 level first voltage source is double of second voltage source and in the third mode 9 level the first voltage and second voltage source is equal and in the fourth position the first voltage source is 2/3 of second voltage source. The capacitor is C1 is used and the resistance R1 is used for DC circuit



Level 1



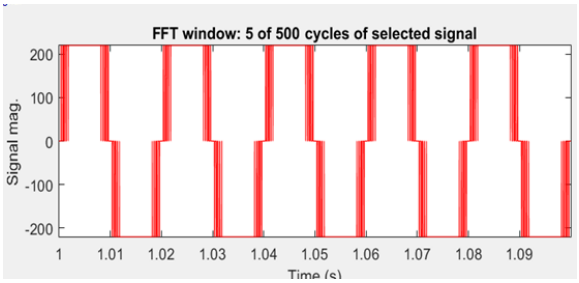
Level 2

Fig.2 Levels of Planned Topology

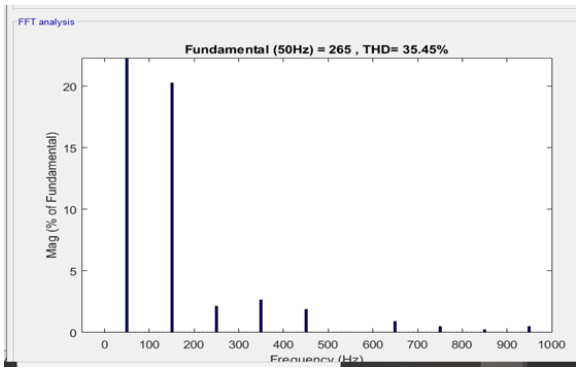
evaluate total number of component count, the topology-I is compared with classical topologies for nine-level output & summarised in Table 2. Core power switches: proposed topology-I in symmetrical configuration achieves 56.25% (7 instead of 16) lessening in the number of main power switches essential as compared with standard topologies. Power diodes: The proposed topology-I in symmetrical configuration attains 37.5% (10 instead of 16) lessening in the number of diodes essential as compared with FC and CHB, whereas % of lessening rises to 86.11% (10 instead of 72) as related with NPC. Similarly, it achieves 74% (2 instead of 8) lessening in number of capacitor compulsory when associated with the NPC and 94.44% (2 instead of 36) lessening when compared with the FC. The different operating modes & switching states along with equivalent output voltage levels for nine level inverter are summarised in Fig. 2 and Table 3, respectively. Similarly, different switching states of topology-I in asymmetrical configuration for synthesising 7-level and 11-level are summarised in Tables 4 & 5, respectively. generalisation of topology-I in symmetrical configuration for N level output is assumed as Total number of controlled switches required = (N + 19) 4 4

| Levels | ON state Switches |
|---|---|
| 1 | S5, S1, S3 |
| 0 | Free wheel |
| 2 | S2, S4 |

## III. SIMULATION AND EXPERIMENTAL RESULTS

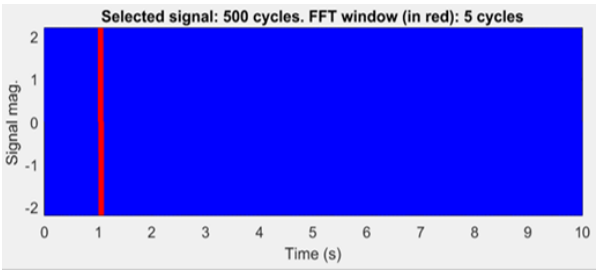



(a)

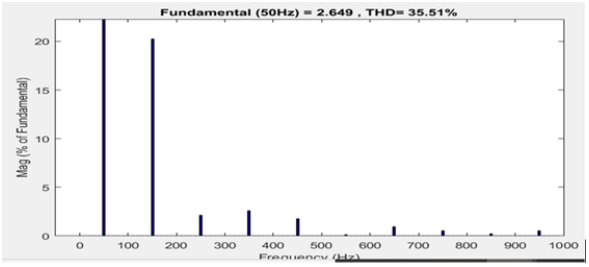



(b)

Fig 3(a)Voltage waveform (b) THD analysis of voltage




(a)




(b)

Fig4 (a) Waveform of current (b) THD analysis of current

*Simulation result is shown in figure 1 and 2 total harmonic distortion are in figure 1 having voltage 35.45% and total harmonic distortion of current is 35.51%*

## CONCLUSION

The Hybrid type topology is used for three level inverter and this can be used Three level inverter has less distorted wave and output is mostly sinusoidal having total harmonic distortion. this topology uses a smaller number of switches of IGBT

## REFERENCES

[1] Hasukh s PATEL RICHARD G. HOFT "Generalized Techniques of Harmonic Elimination & Voltage Control in Thyristor Inverters: Part I1-Voltage Control Techniques" IEEE Transection on industrial applications September/October 1974.

[2] AKIRA NABAE, ISAO TAKAHASHI, HIROFUMI AKAGI "A New Neutral-Point-Clamped PWM Inverter" IEEE Transections on industry applications Volume IA-17 N.5 September/October 1981.

[3] PRADEEP M, V. R. STEFANOVIC, "A Versatile Commutation Circuit for PWM Inverters" IEEE Transections on industry applications Volume IA-18 No.2 March/April 1982.

[4] PRADEEP M, V. R. STEFANOVIC "Generalized Structure of a Multilevel PWM Inverter" IEEE Transections on industry applications Volume IA-19 No.6 November/December 1983.

[5] Giuseppe Carrara, , Simone Gardella, Mario Marchesoni, Raffaele Salutari, & Giuseppe Sciutto "A New Multilevel PWM Method: A Theoretical Analysis" IEEE Transections on Power Electronics Vol.7 No.3 July 1992.

[6] Leon M. Tolbert, Thomas G. Habetler, "Novel Multilevel Inverter Carrier Based PWM Method" IEEE Transections on industry applications Volume 35 No.5 September/October 1999.

[7] Brendan Peter McGrath, Donald Grahame Holmes "Multicarrier PWM Strategies for Multilevel Inverters" IEEE Transections on industrial Electronics Volume 49 No.4 August 2002.

[8] Juan Dixon, Luis Morán "High-Level Multistep Inverter Optimization Using a Minimum Number of Power Transistors" IEEE

Transections on industrial Electronics Volume 21 No.2 March 2006.

[9] Zhou Jinghua, Li Zhengxi, "Research on Hybrid Modulation Strategies Based on General Hybrid Topology of Multilevel Inverter" Speedam 2008 978-1-4244-1664-6/08 IEEE

Alireza Nami, Firuz Zare, Arindam Ghosh, Frede Blaabjerg, "A Hybrid Cascade Converter Topology with Series Connected

[10] Symmetrical & Asymmetrical Diode Clamped H Bridge Cells" IEEE Transections on Power Electronics Vol.26 No.1 January 2011.

[11] P. Palanivel, S.S. Dash, "Analysis of THD & output voltage performance for cascaded multilevel inverter using carrier PWM techniques" IET Power Electron., 2011, Vol. 4, Iss. 8, pp. 951–958.

[12] K k gupta, S. Jain "Topology for multilevel inverters to attain maximum number of levels from given DC sources" ET Power Electron., 2012, Vol. 5, Iss. 4, pp. 435–446.

[13] Ehsan Najafi, Abdul Halim Mohamed Yatim "Design & Implementation of a New Multilevel Inverter Topology" IEEE Transections on industrial Electronics Volume 59 No.11 November 2012.

[14] Raul Rebinoviece, Dmitry Baimel, Jacek Tomasik, Adrian Zuckerberger "Thirteen-level cascaded H-bridge inverter operated by Generic phase shifted pulse-width modulation" IET Power Electron., 2013, Vol. 6, Iss. 8, pp. 1516–1529

[15] Arif Al judi, Edwin Nowicki "Cascading of diode bypassed transistor-voltage source units in multilevel inverters" IET Power Electron., 2013, Vol. 6, Iss. 3, pp. 554–560

[16] Ali Ajami, Mohammad Reza Jannati Oskuee, Ataollah Mokhberdoran, Alex Van den Bossche "Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stresses of switches" IET Power Electron., 2014, Vol. 7, Iss. 2, pp. 459–466

[17] Rasoul Shalchi Alishah, Daryoosh Nazarpour, Seyed Hossein Hosseini, Mehran Sabahi "Novel Topologies for Symmetric, Asymmetric, and Cascade Switched-Diode Multilevel Converter With Minimum Number of Power Electronic Components" IEEE Transections on industrial Electronics Volume 61 No.10 October 2014

[18] Ebrahim Babaei, Saeed Sheer mohammad zadeh Gowgani "Hybrid Multilevel Inverter Using Switched Capacitor Units" IEEE Transections on industrial Electronics Volume 61 No.9 September 2014

[19] Mahrous Ahmed, Ahmed Sheir, Mohamed Orabi "Real-Time Solution and Implementation of Selective Harmonic Elimination of Seven-Level Multilevel Inverter" IEEE Journal of emerging and Selected Topics in Power Electronics, Vol. 5, NO. 4, December 2017

[20] Ahmed Salem, Huynh Van Khang, Kjell G. Robbersmyr "New Multilevel Inverter Topology with Reduced Component Count" ISBN: 978-9-0758-1531-3 - IEEE catalog number: CFP19850-ART

[21] Shivam Prakash Gautam, Lalit Kumar, Shubhrata Gupta "Hybrid topology of symmetrical multilevel inverter using less number of devices" IET Power Electron., 2015, Vol. 8, Iss. 11, pp. 2125–2135